

PEGATRON CONFIDENTIAL

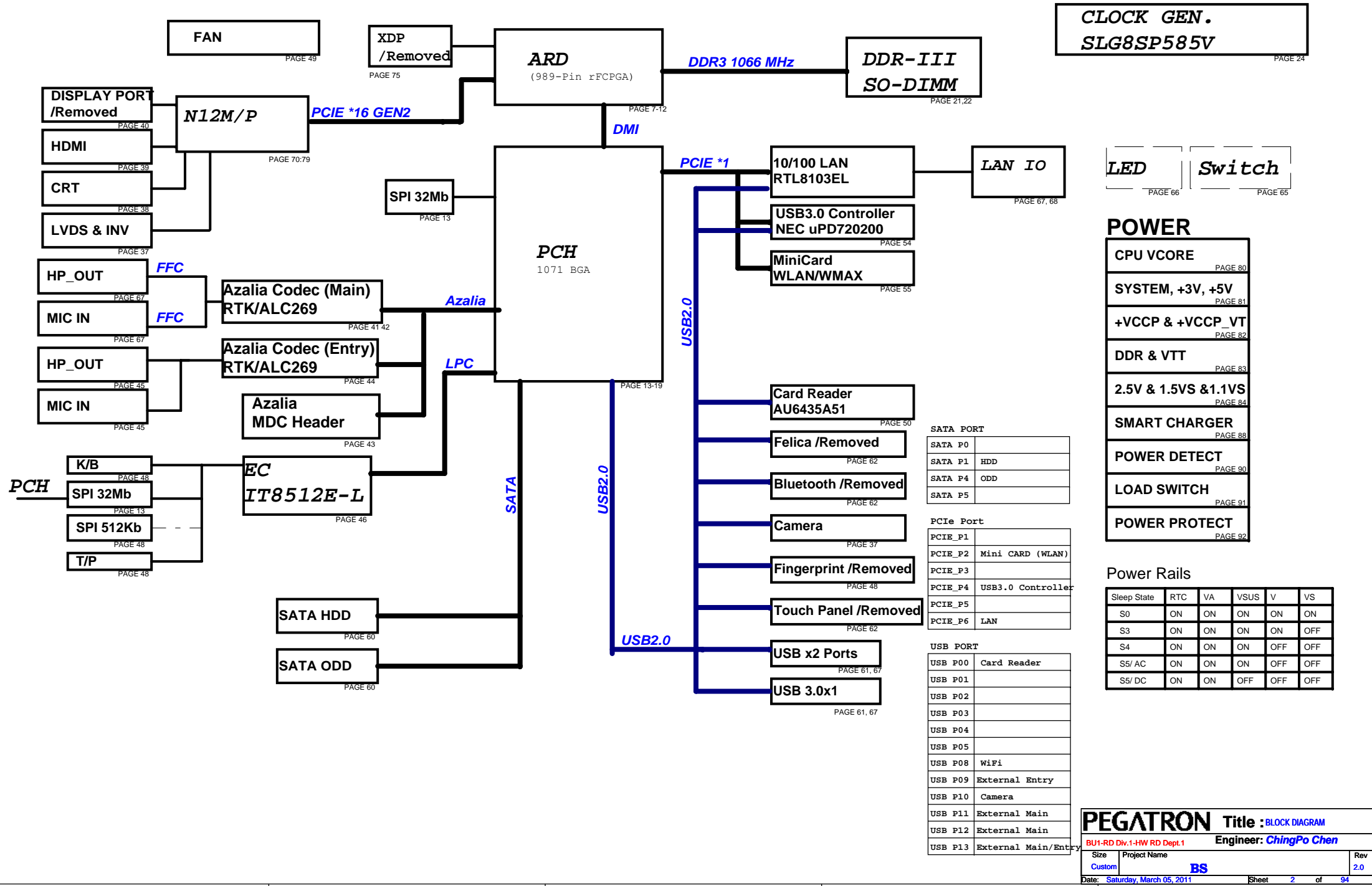
MODEL NAME :

PCB NO :

69- P/N :

BS/TK Colay Schematic  
Intel Arrandale rPGA-989  
PCH BGA 1071  
2010-07-19  
REV :R1.0

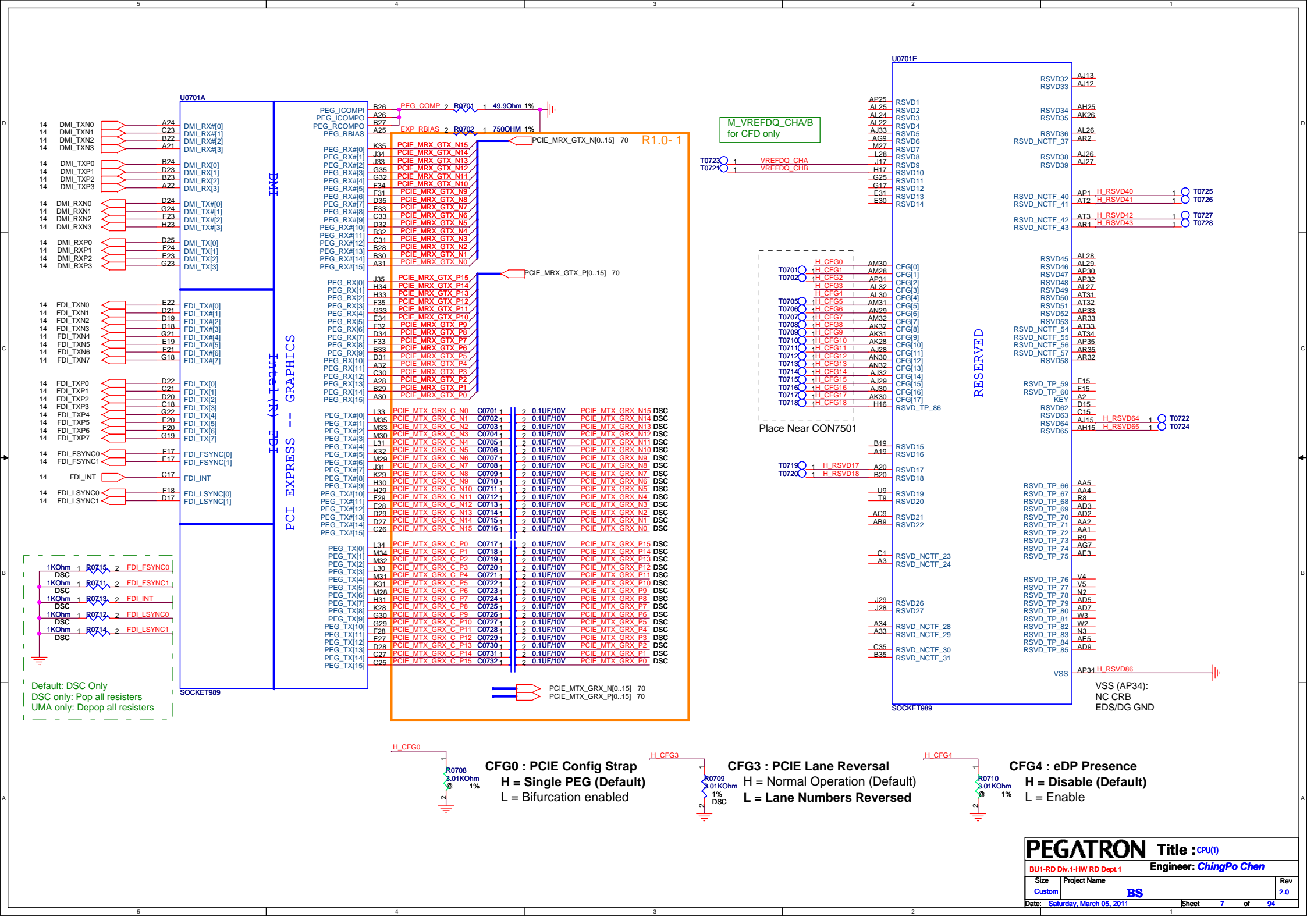
# BS/TK BLOCK DIAGRAM

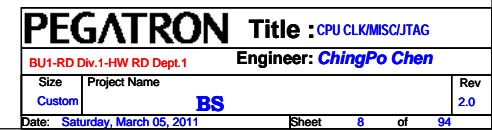


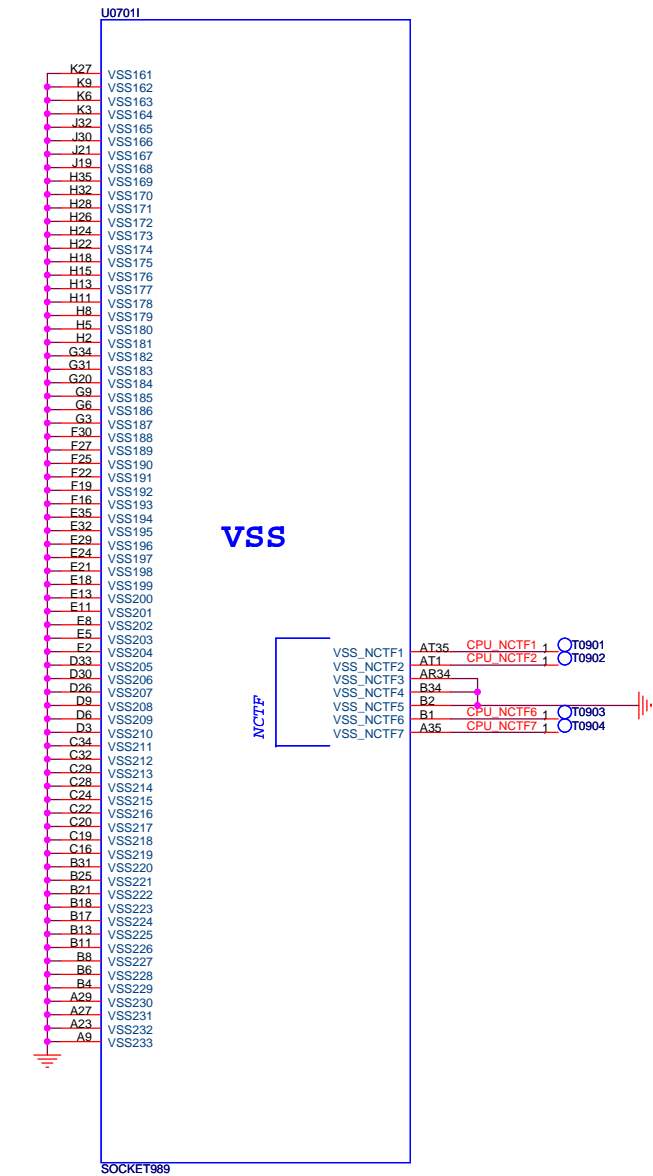
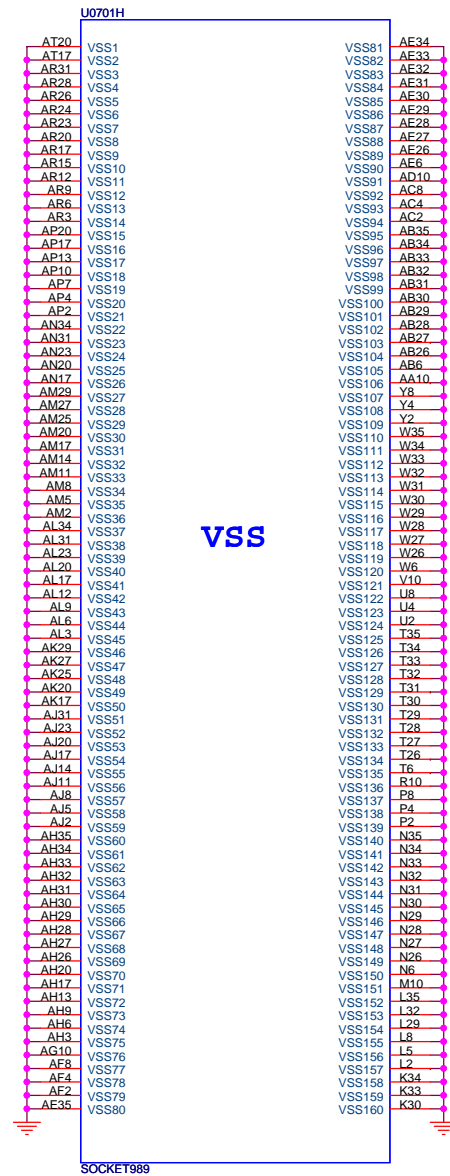
# SCHEMATIC INDEX V1.0

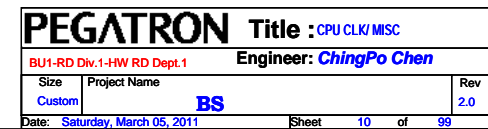
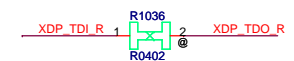
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PAGE#	Description	NOTE
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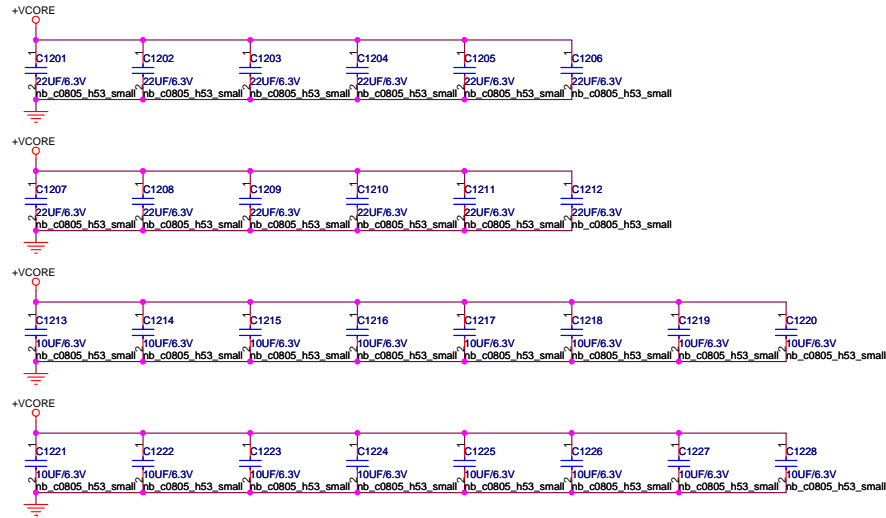


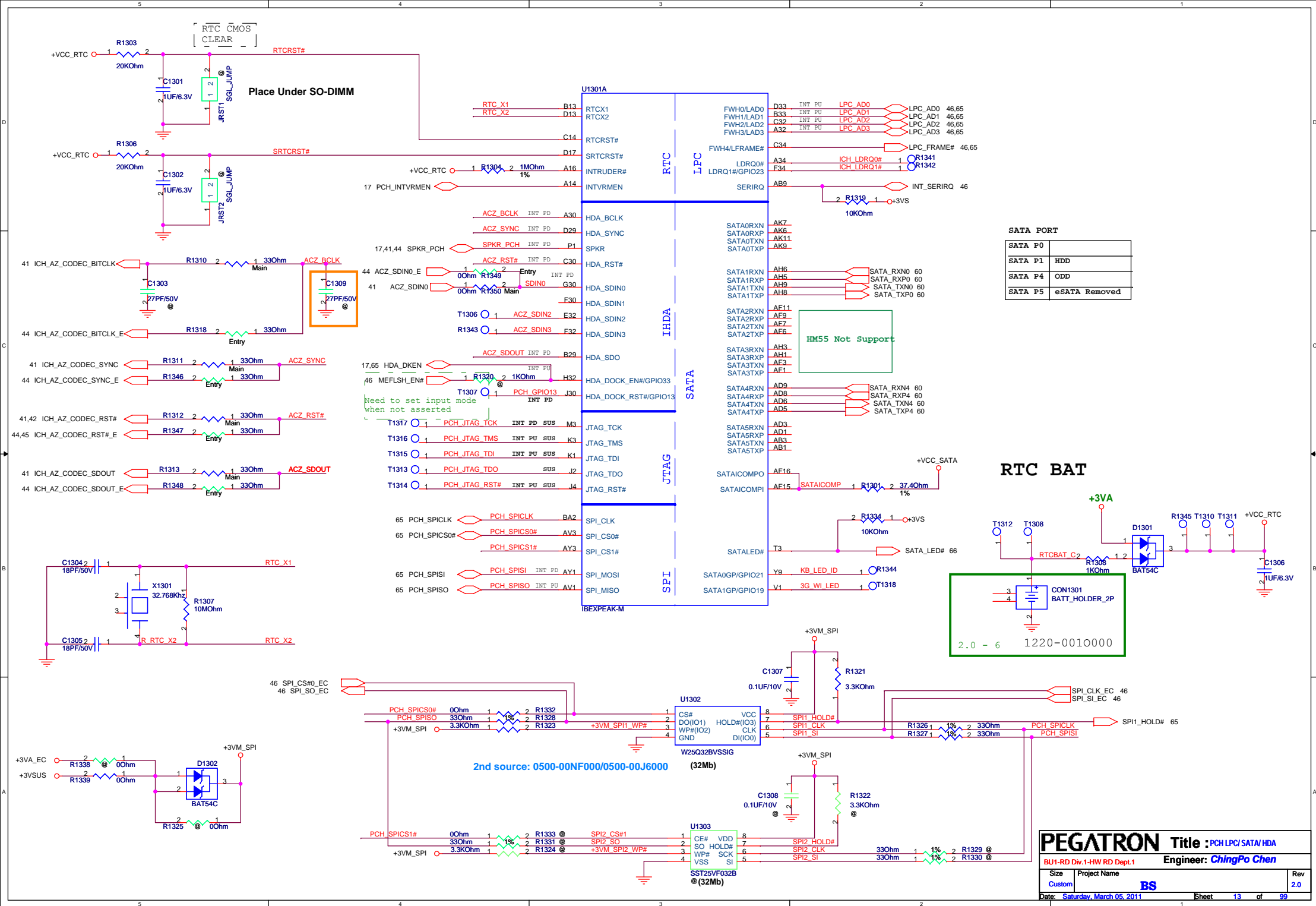


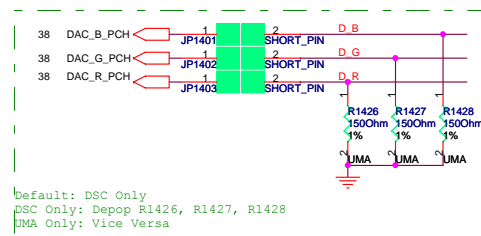
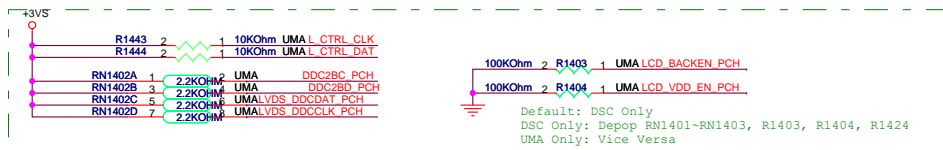
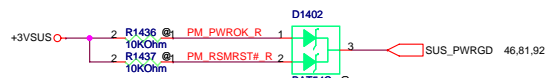


Decoupling guide from INTEL

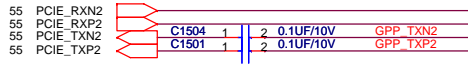
VCORE	10uF	x 16pcs
	22uF	x 12pcs



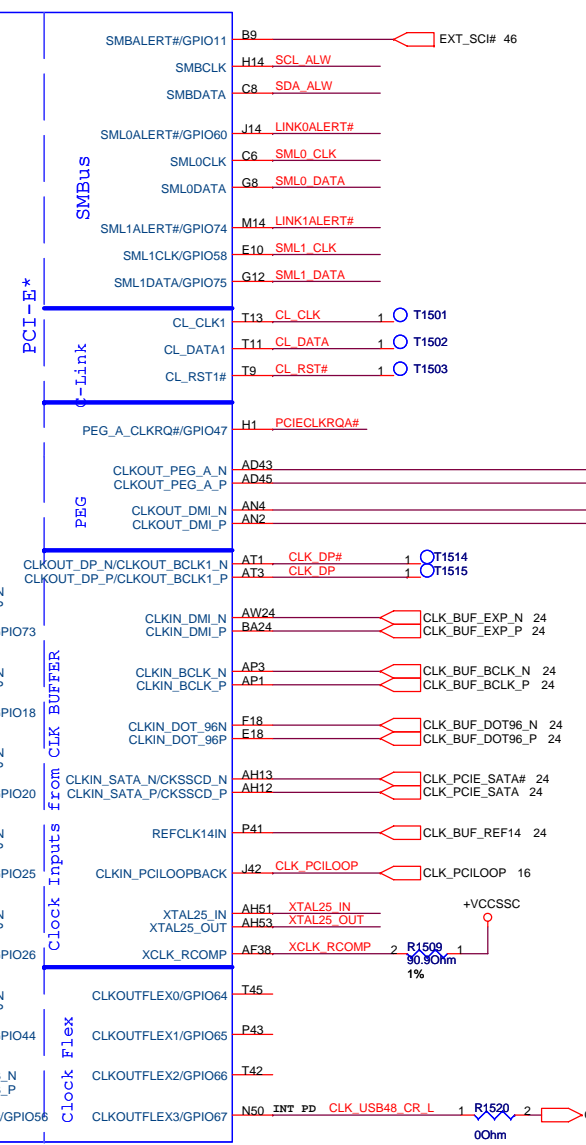
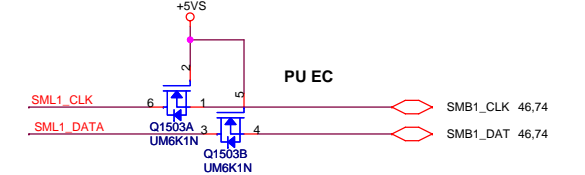
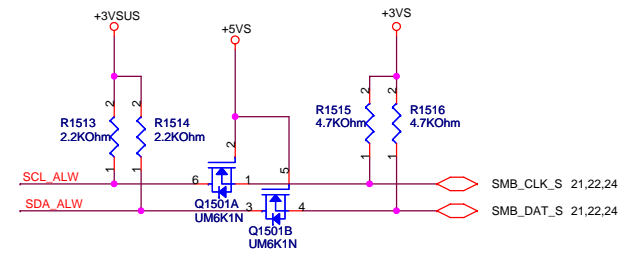
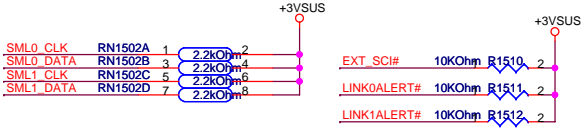
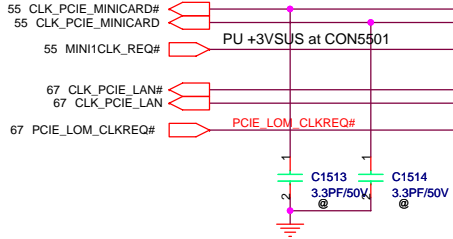
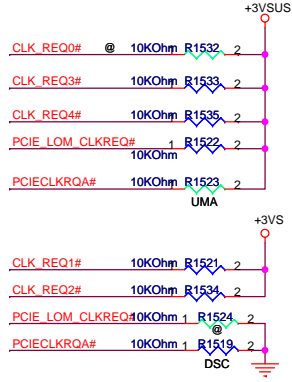




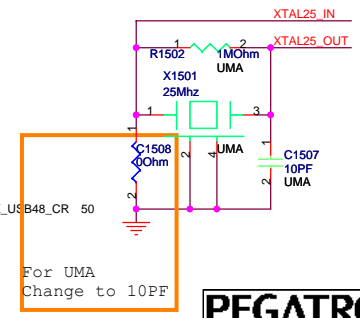
PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	LAN



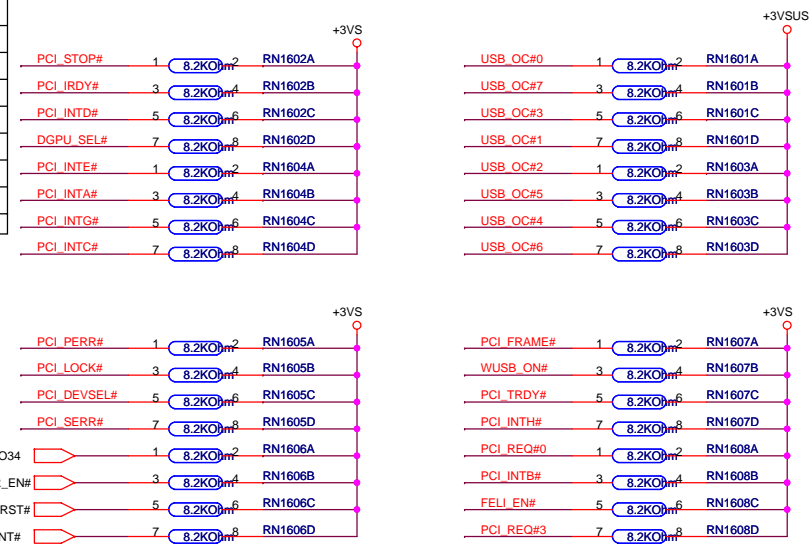
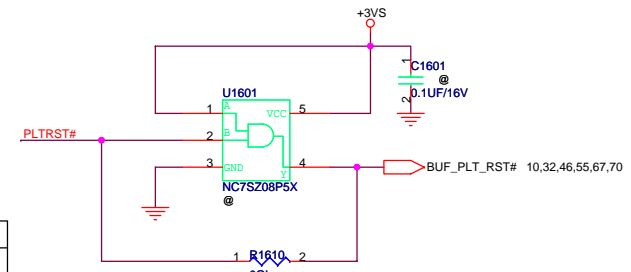
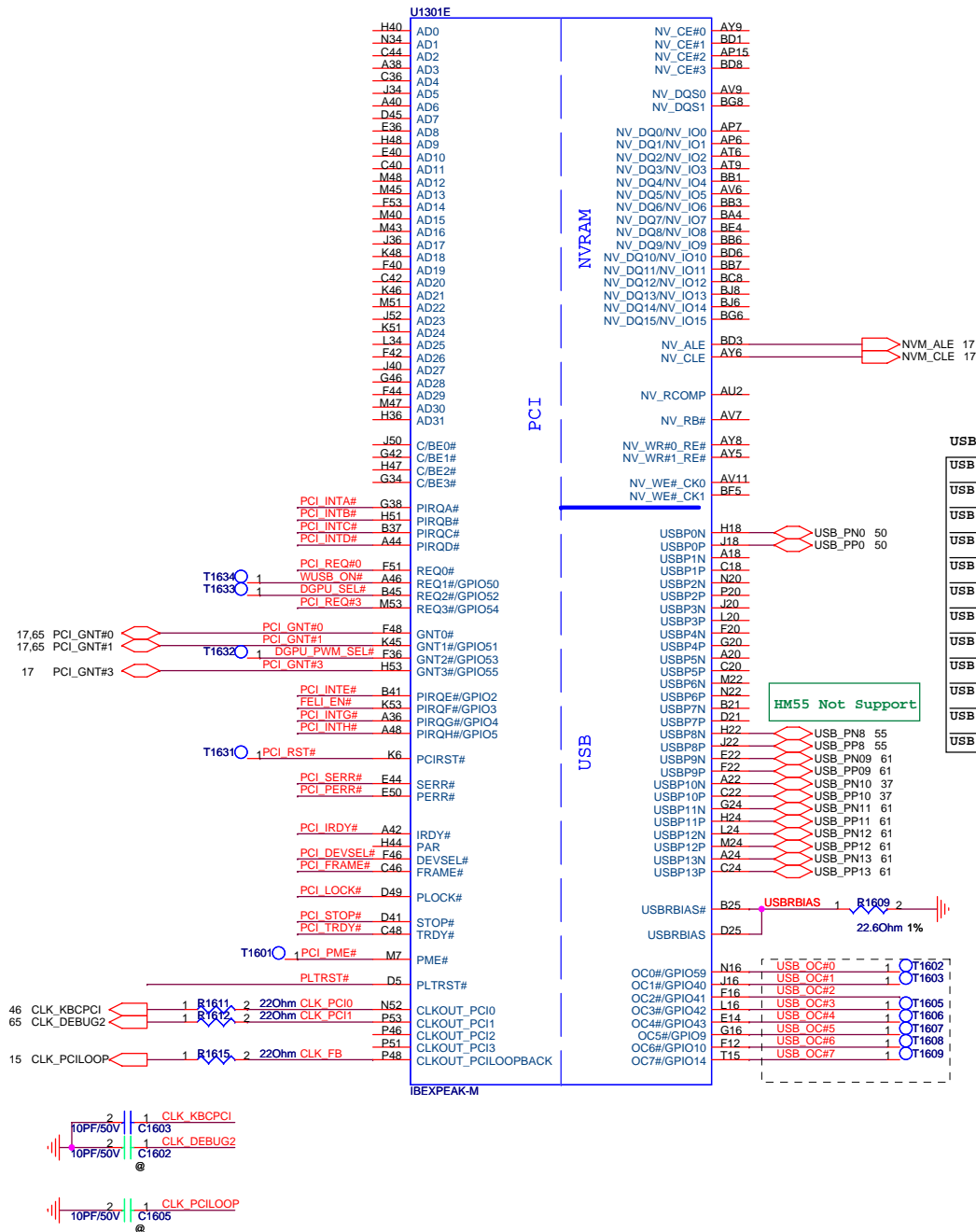
HM55 Not Support

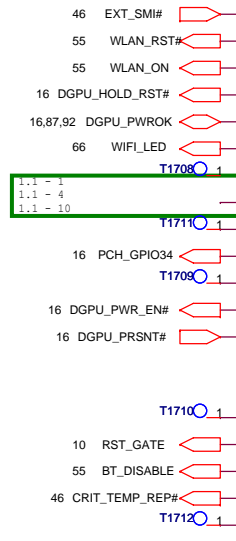
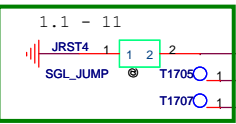


Damping CPU Side

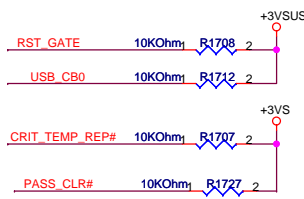
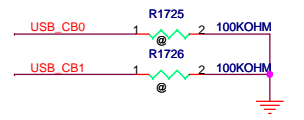
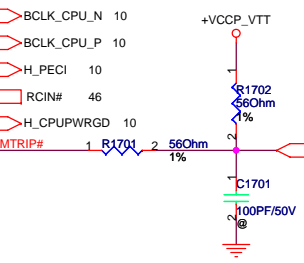
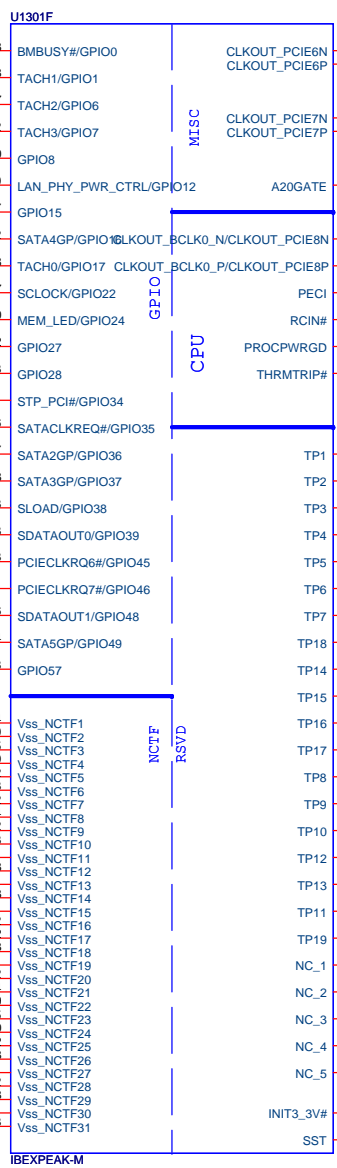
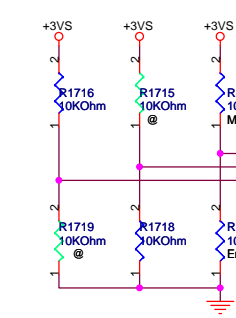


For UMA  
Change to 10PF

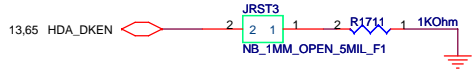




PCB_VID	0	1	2
E 1.0	0	0	0
E 1.1	0	0	1
E 2.0	0	1	0
M 1.0	1	0	0
M 1.1	1	0	1
M 2.0	1	1	0



HDA\_DKEN : Flash Descriptor Security Override  
H = Disabled (Default)  
L = Enabled  
**Note : Rising edge of PWROK**



**NOTE:**  
Assert the HDA\_DKEN will halt and disable Intel ME.  
This is a debug mode and must not asserted after manufacturing/debug.

PCH\_SPI1 : iTPM STRAP  
H : Enable iTPM  
L : Disable iTPM (Default)

Description Only.  
No PU Reserved

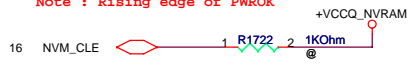
PCI\_GNT#3 : A16 swap override  
Strap/Top-Block Swap Override jumper  
H : Default  
L : A16 swap override/Top-Block Swap  
Override enabled

**Note : Rising edge of PWROK**



NVM\_CLE : DMI Termination Voltage  
H : Set to Vcc  
L : Set to Vss

**Note : Rising edge of PWROK**

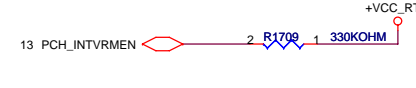


GPIO15/ WLAN\_ON :  
H = Intel ME Crypto Transport Layer Security (TLS)  
cipher suite with confidentiality  
L = Intel ME Crypto Transport Layer Security (TLS)  
cipher suite with no confidentiality

**Note : Rising edge of RSMRST# pin**



PCH\_INTVRMEN : Integrated SUS 1.05V VRM Enable  
H : Integrated VRM is enabled  
L : Integrated VRM is disabled  
**Note: This signal should always be pulled high**



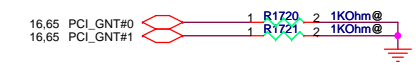
SPKR\_PCH : NO REBOOT STRAP  
H : Enable  
L : Disable (Default)  
**Note : Rising edge of PWROK**



PCI\_GNT#1, PCI\_GNT#0 : Boot BIOS Strap

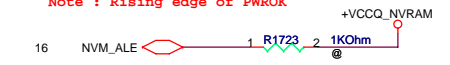
PCI_GNT#0	PCI_GNT#1	
0	0	LPC
0	1	PCI
1	1	SPI

**Note : Rising edge of PWROK**



NVM\_ALE : Danbury Technology Enabled  
High--> Enable Intel Anti-Theft Technology.  
Low--> Disable Intel Anti-Theft Technology.

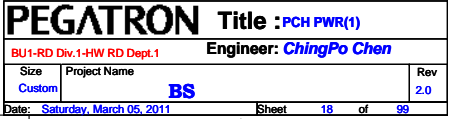
**Note : Rising edge of PWROK**



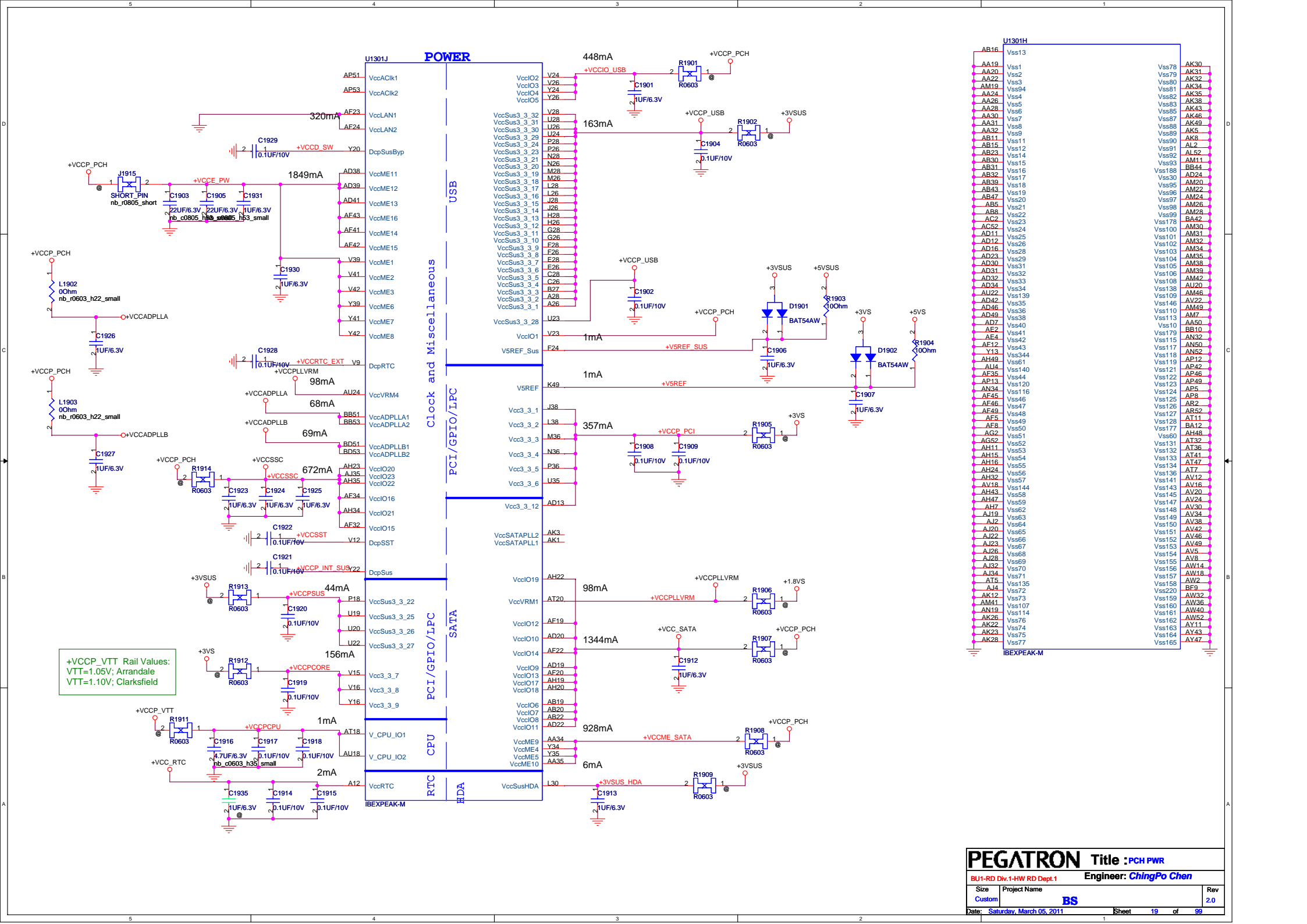
GPIO27/ USB\_SW :  
H = Enables the internal VccVRM. (Default)  
L = Disables the VccVRM.

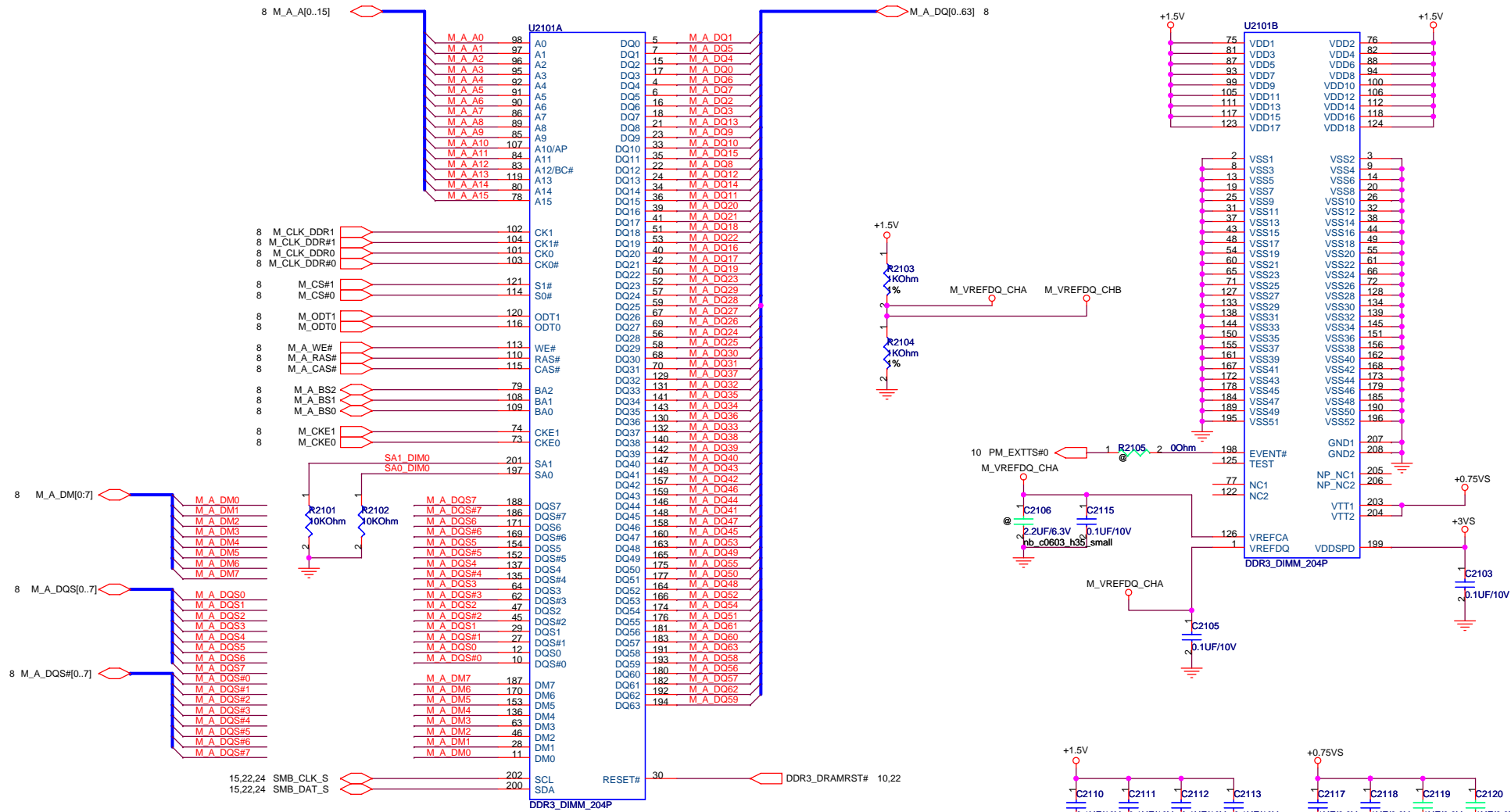
**Note : Rising edge of RSMRST# pin**











Note:  
 If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
 SO-DIMMA SPD Address is 0xA0  
 SO-DIMMA TS Address is 0x30  
 If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
 SO-DIMMA SPD Address is 0xA2  
 SO-DIMMA TS Address is 0x32

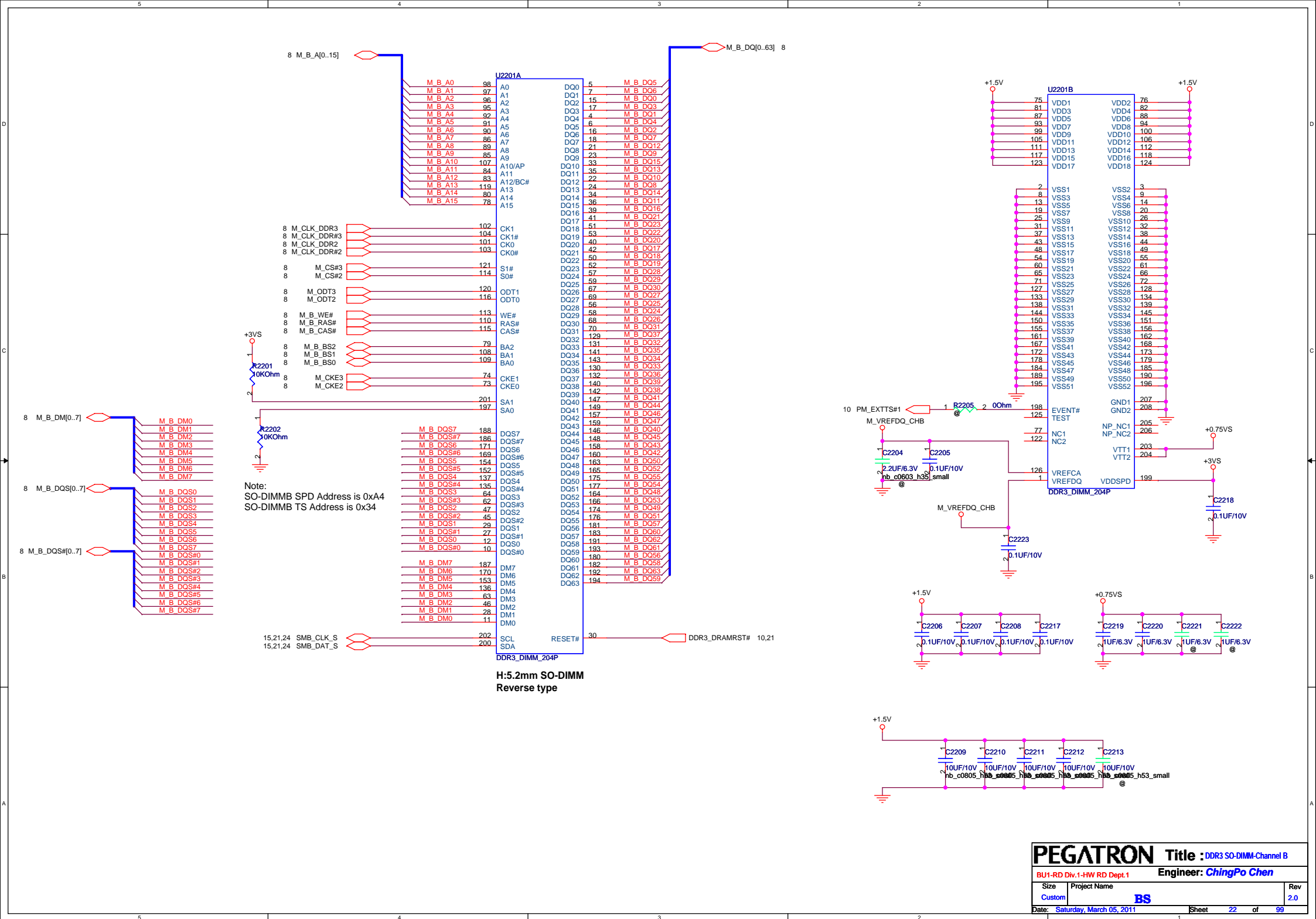
H:9.2mm SO-DIMM  
 Reverse type

**PEGATRON** Title : DDR3 SO-DIMM-Channel A

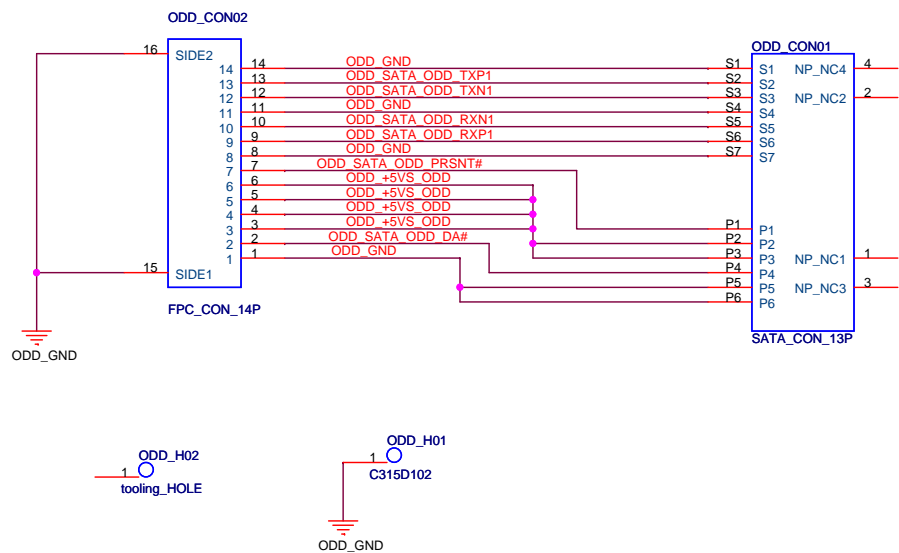
BU1-RD Div.1-HW RD Dept.1 Engineer: **ChingPo Chen**

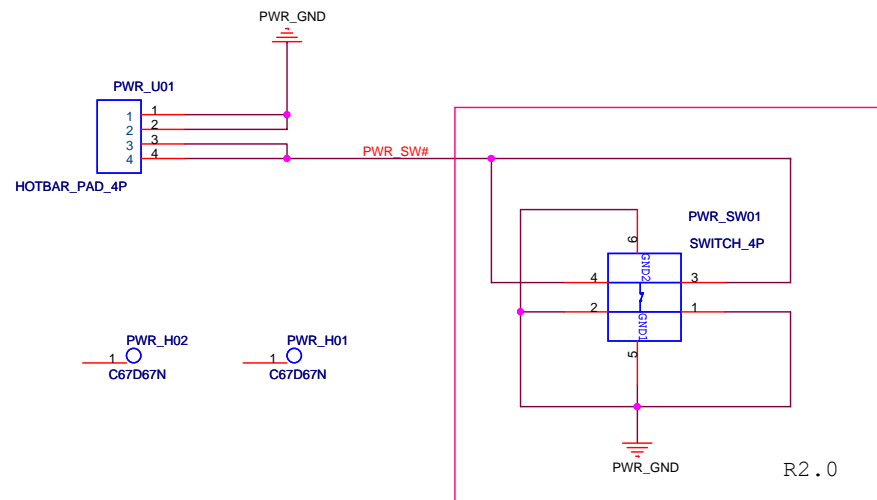
Size Project Name  
 Custom **BS**

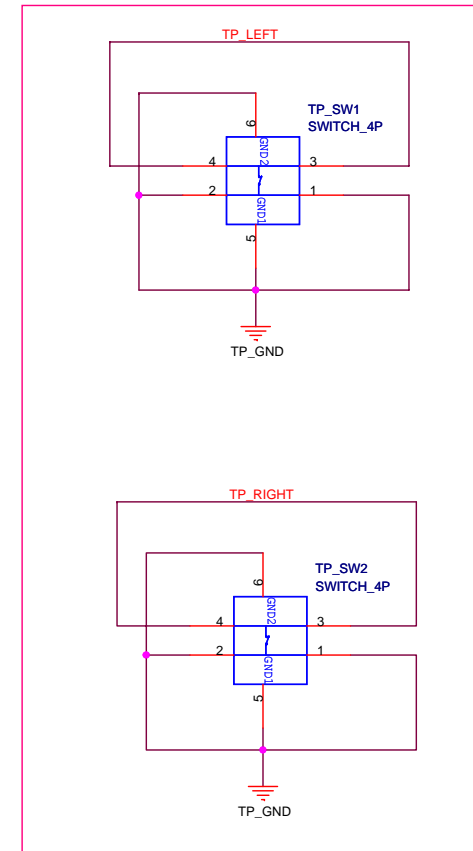
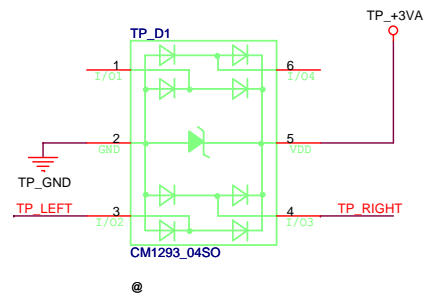
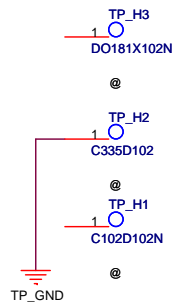
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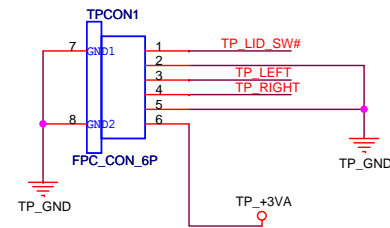
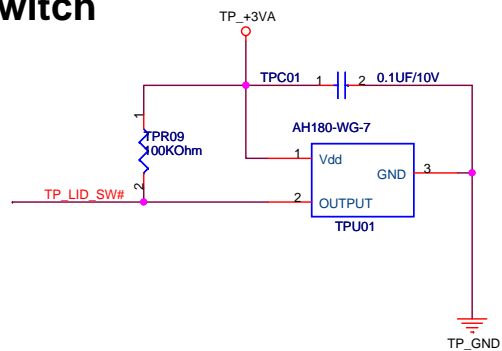






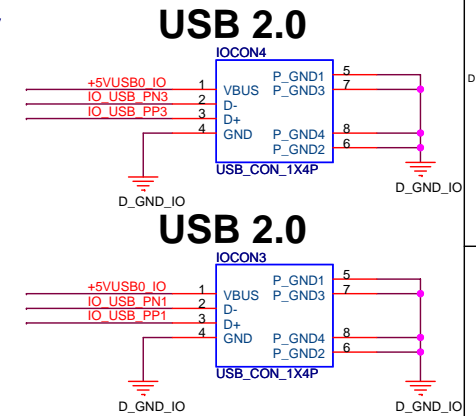
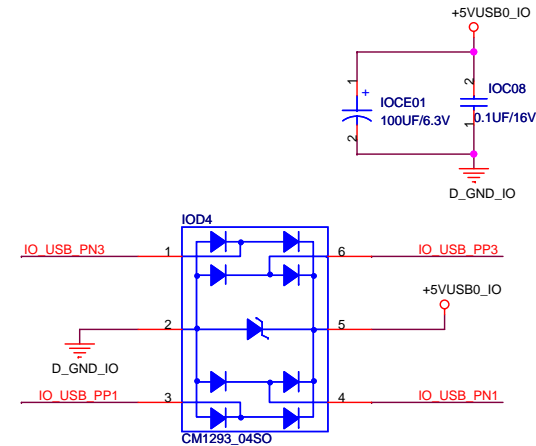
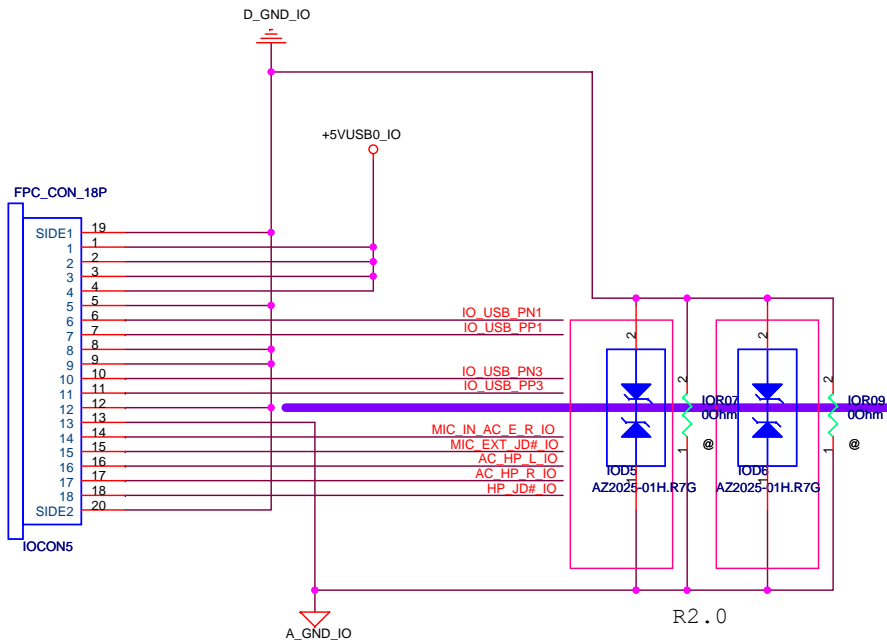
R2.0

## LID Switch

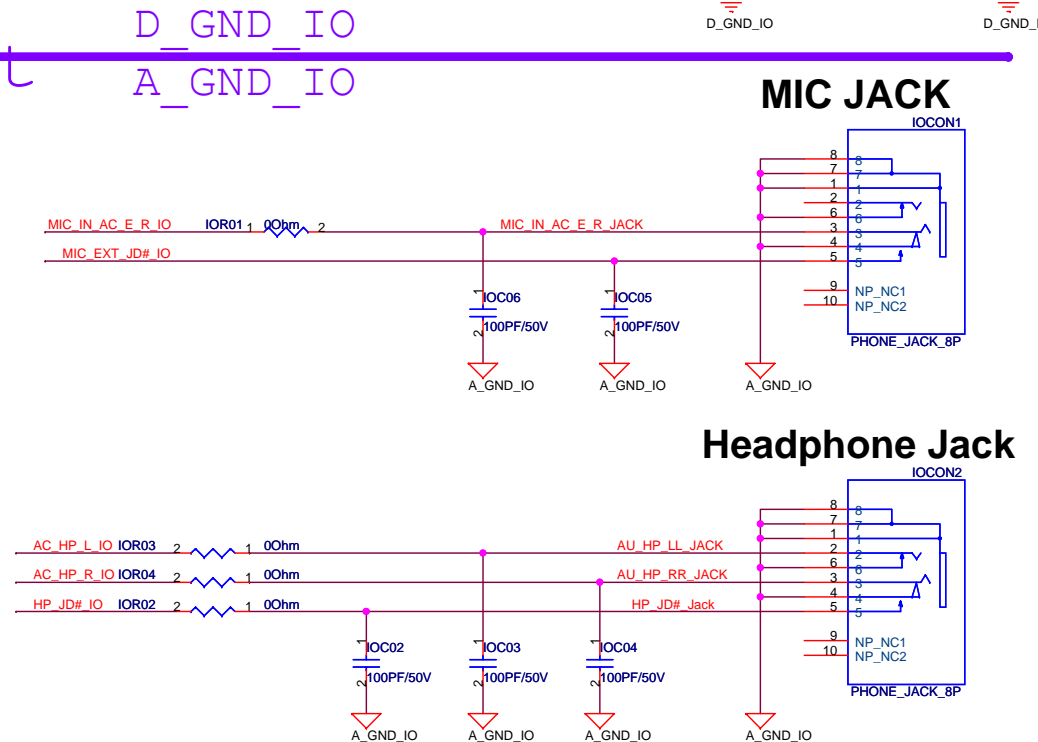
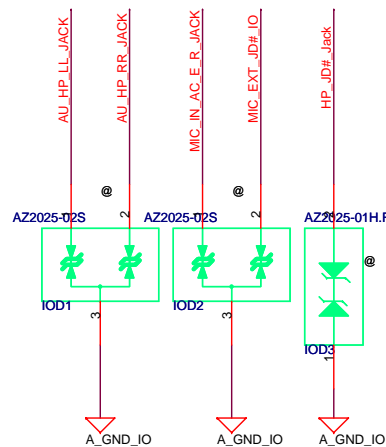
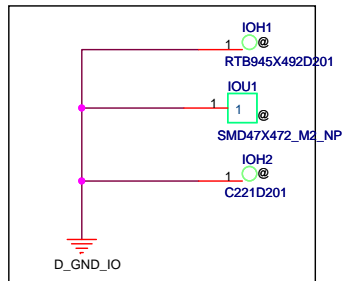


<b>PEGATRON</b>		Title : TP_M	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Stanly Hsu	
Size B	Project Name BS		Rev 2.0
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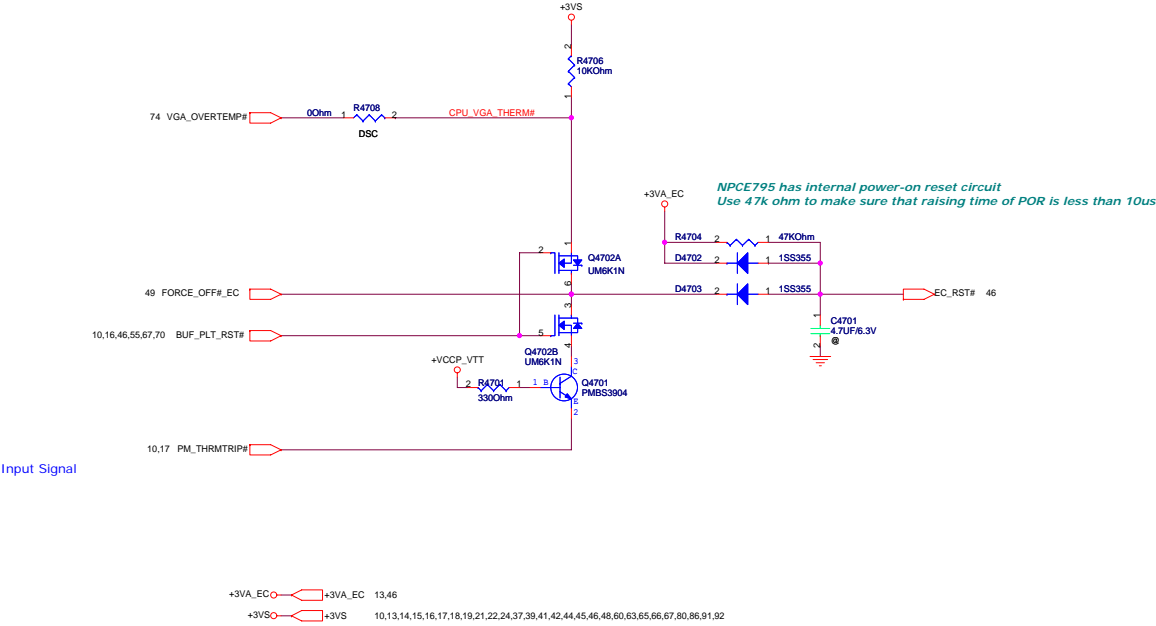


## Ground Hole&Pad

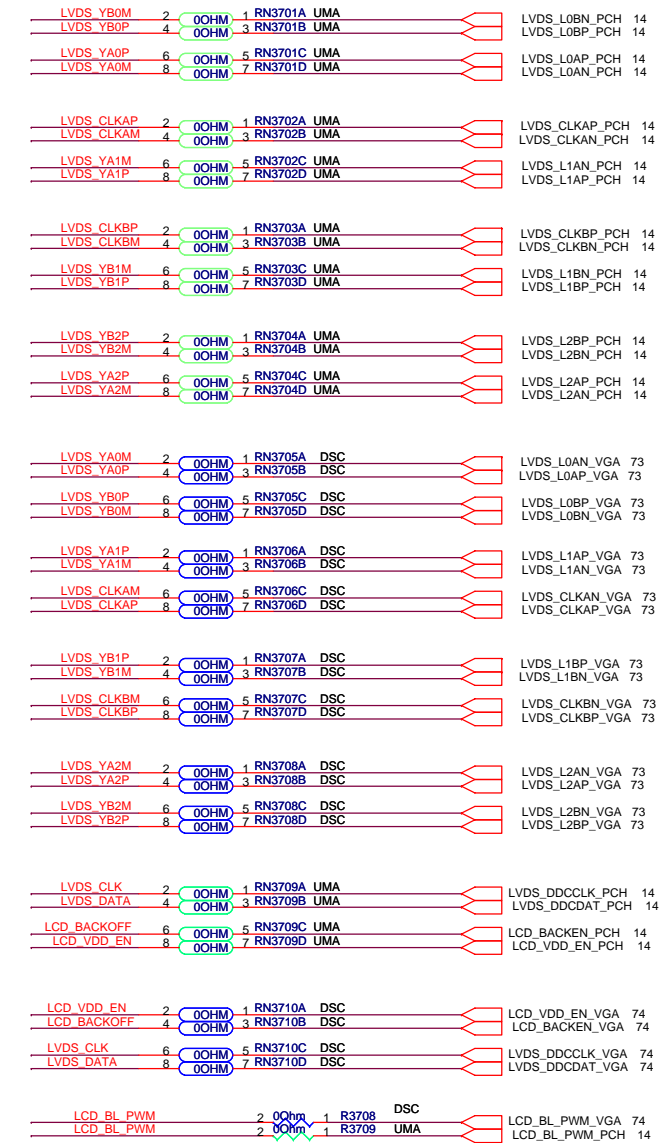
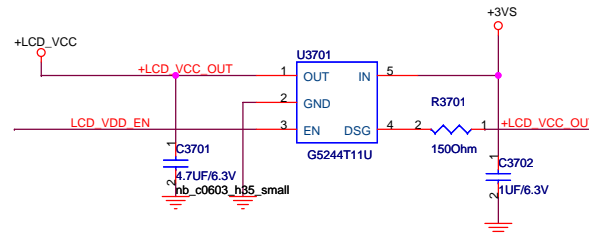
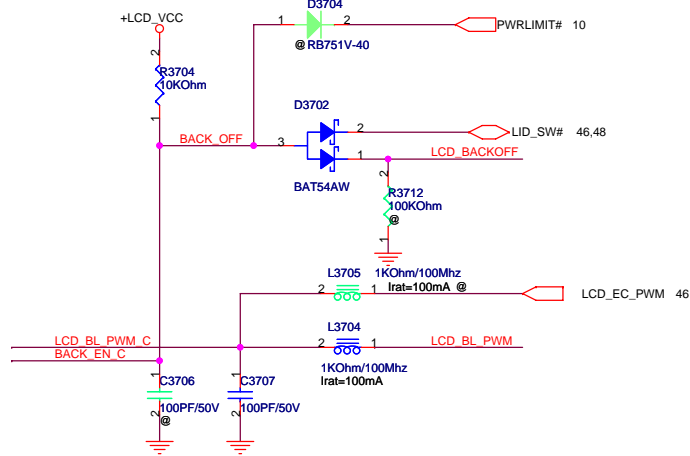
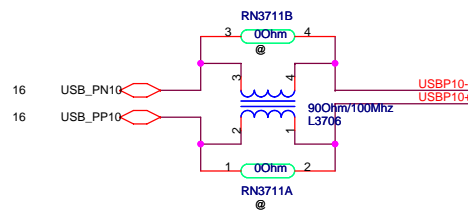
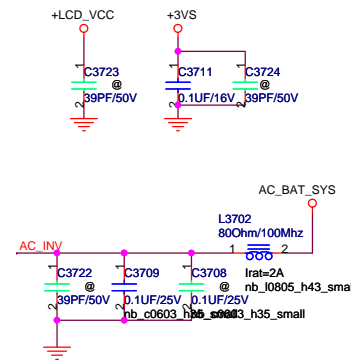
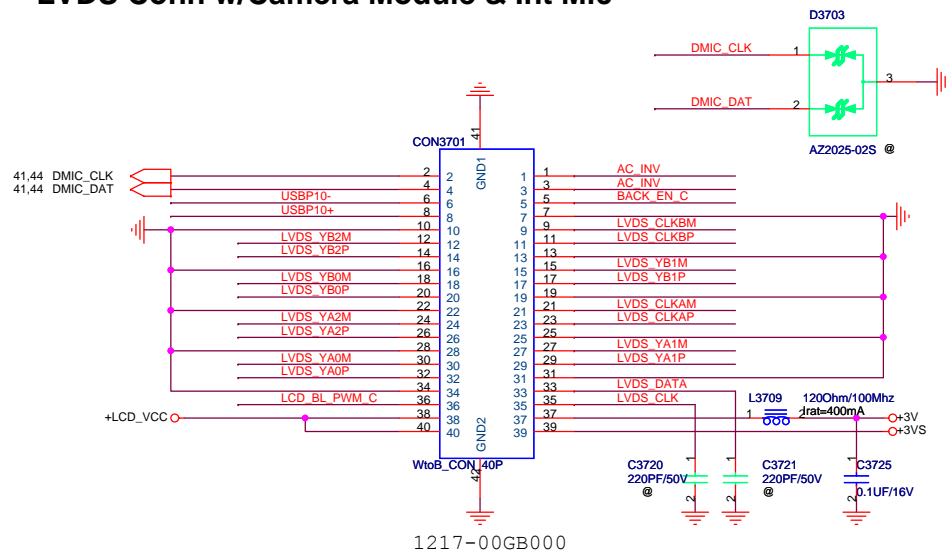


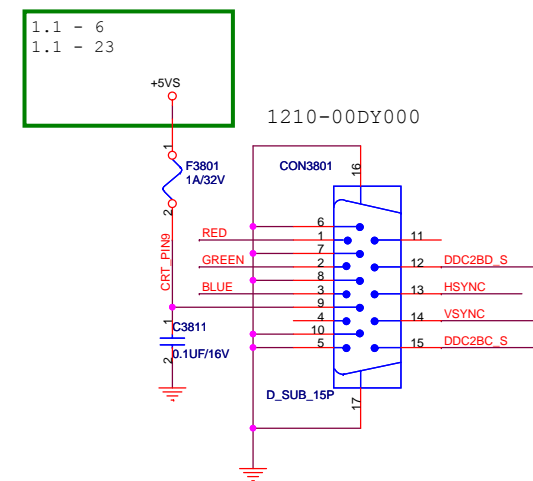
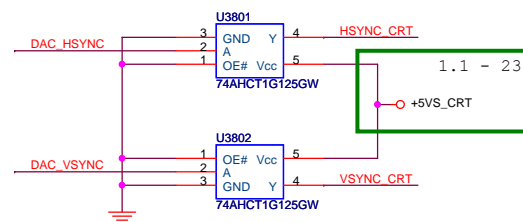
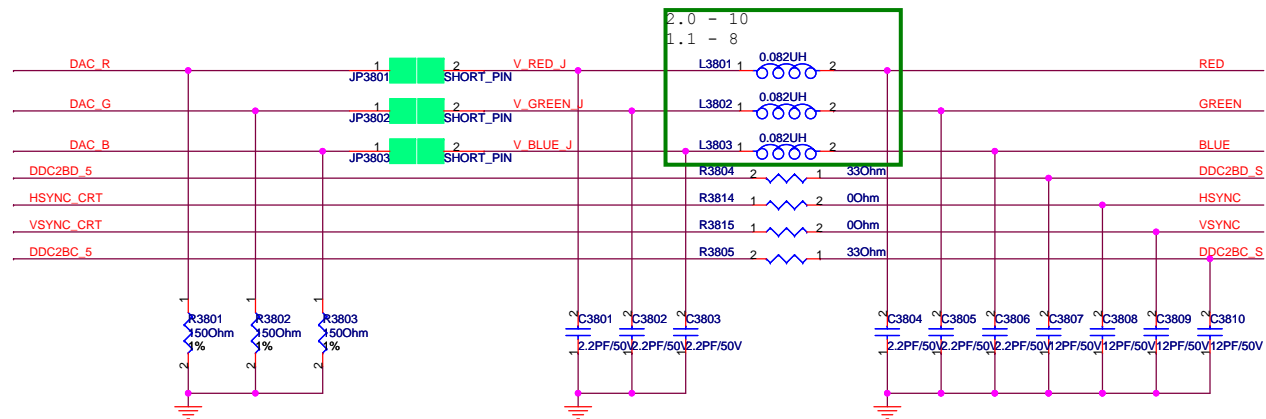
PEGATRON Title : IO		
BG1-NB1-HW-NB5		
Engineer: JR Huang		
Size	Project Name	Rev
B	BS	2.0
Date: Saturday, March 05, 2011	Sheet 28 of 99	

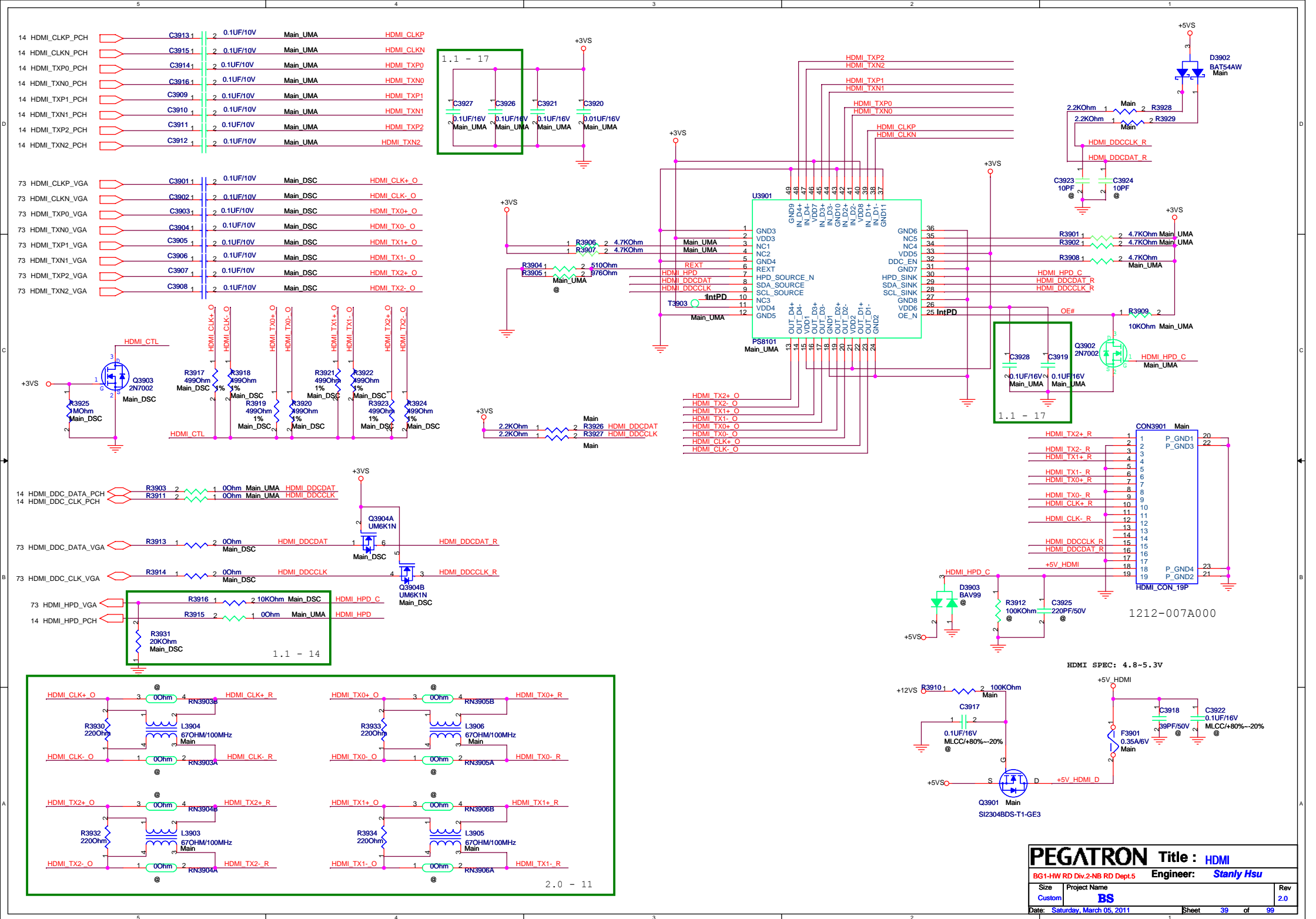
Thermal Policy

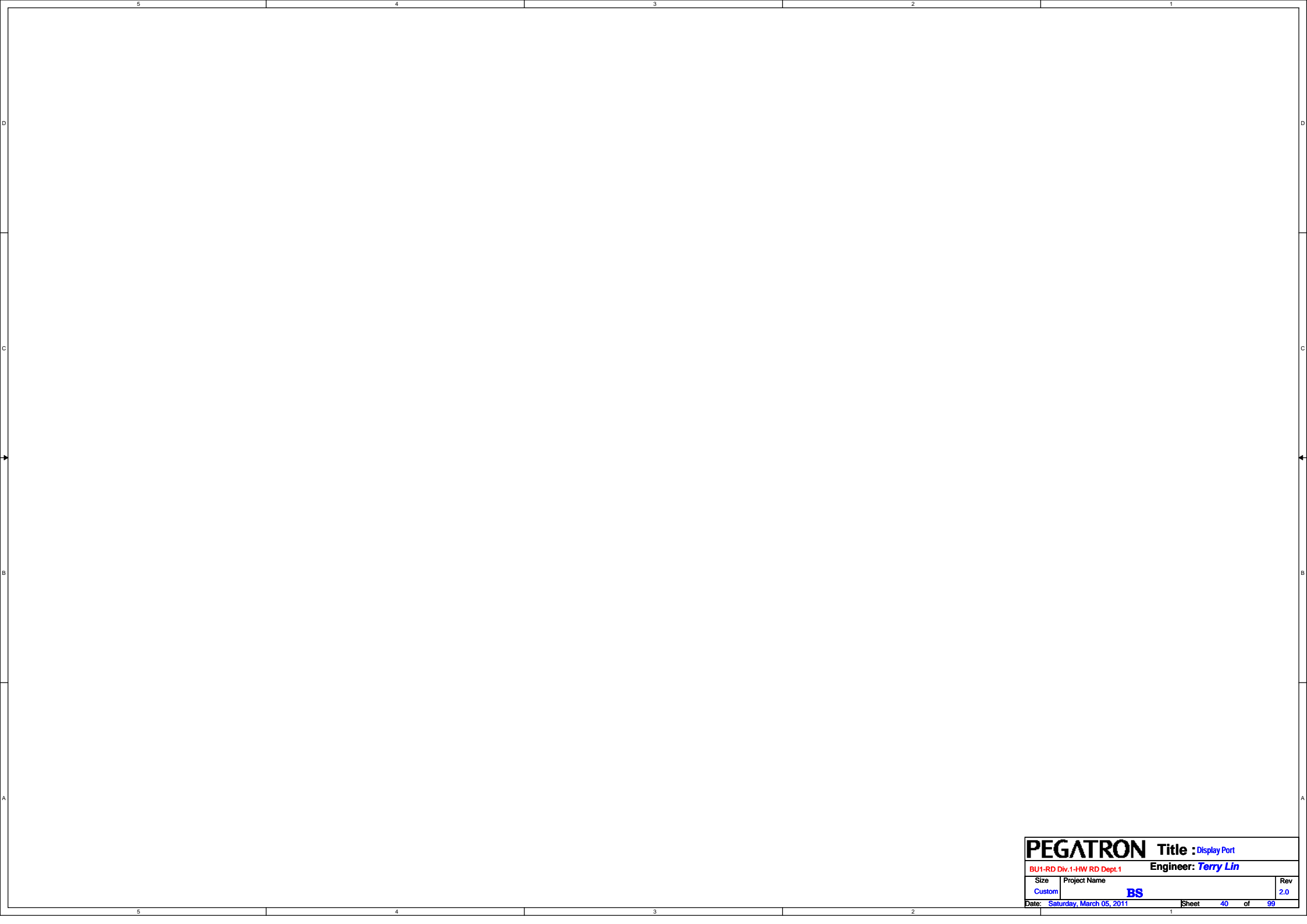


### LVDS Conn w/Camera Module & Int Mic

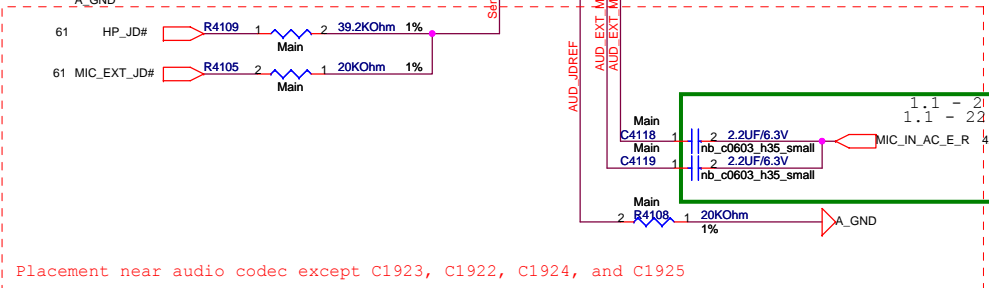
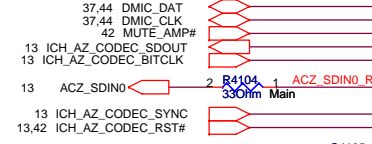
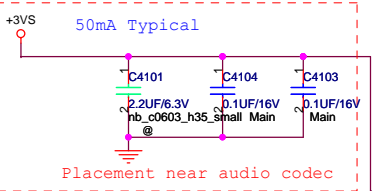
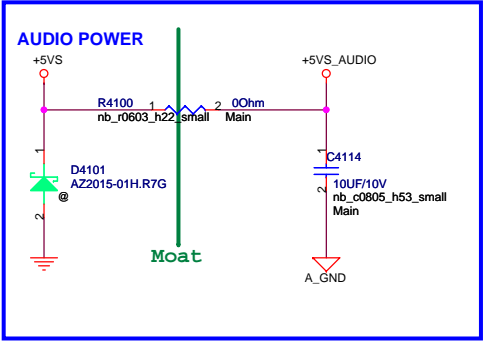
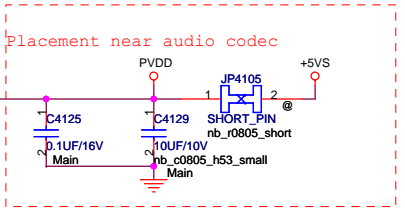
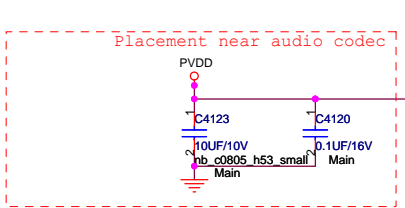
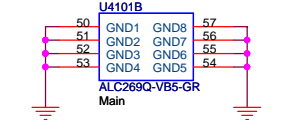
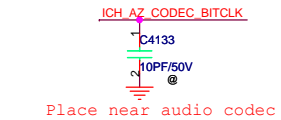
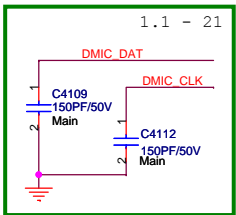






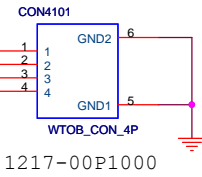
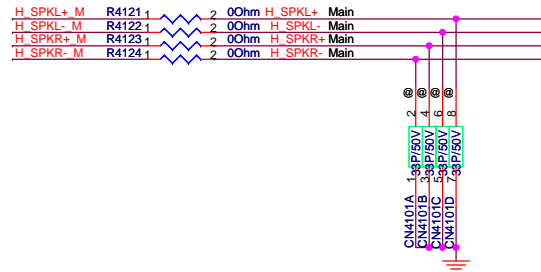
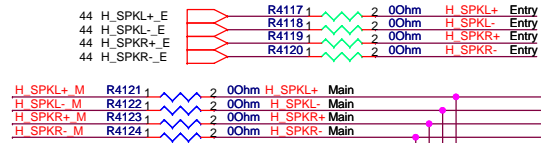
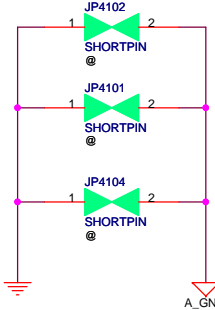


<b>PEGATRON</b>		<b>Title :</b> Display Port	
BU1-RD Div.1-HW RD Dept.1		<b>Engineer:</b> Terry Lin	
Size Custom	Project Name  <b>BS</b>		Rev 2.0
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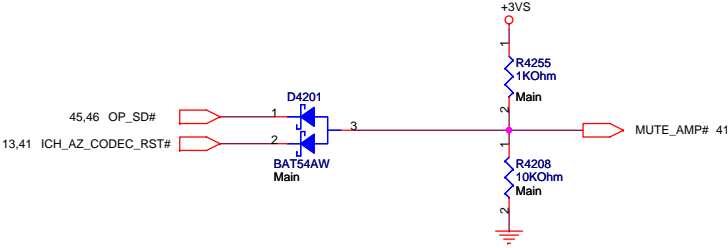
Configuration for ALC269

Internal Speaker: Port D  
External Headphone: Port A  
External Microphone: Port F  
Internal Microphone: Port B





AMP De-Pop Control circuit



41 VREFOUT\_A\_E\_R

1.1 - 2  
1.1 - 22

41 MIC\_IN\_AC\_E\_R

R4204  
1KOhm  
Main

R4210  
4.7KOhm  
Main

MIC\_IN\_AC\_E\_J 61

41 AC\_HP\_R

75Ohm  
R4205 Main  
R4206  
75Ohm Main

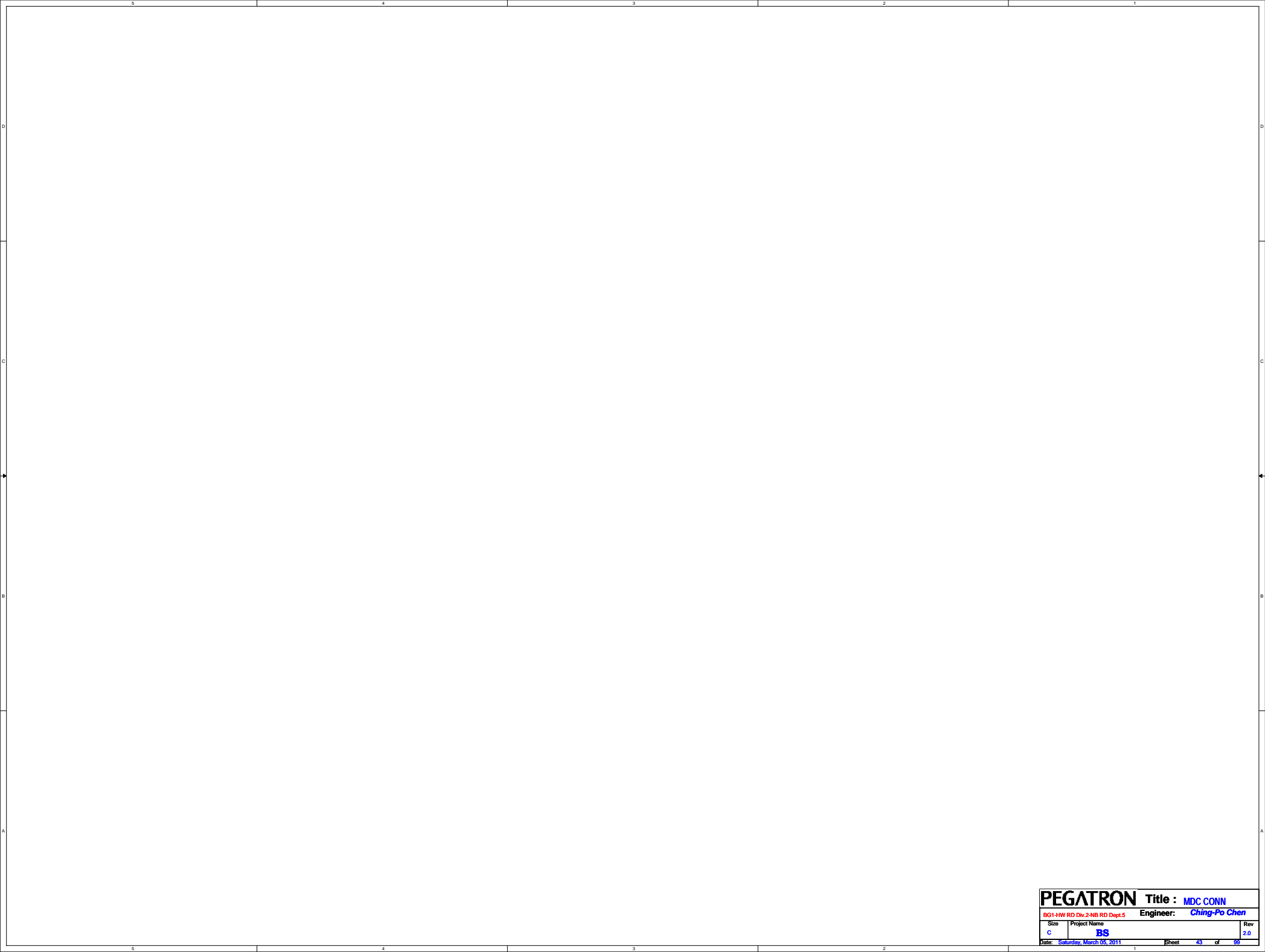
HP JACK\_R

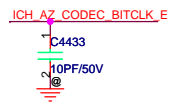
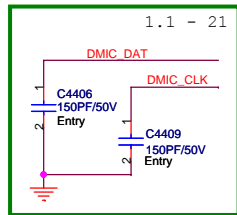
HP JACK\_R 61

41 AC\_HP\_L

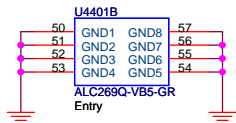
HP JACK\_L

HP JACK\_L 61



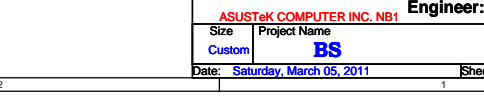
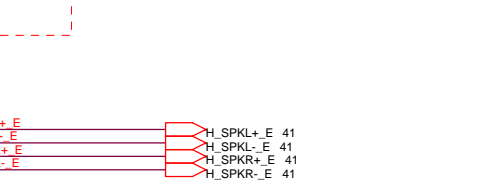
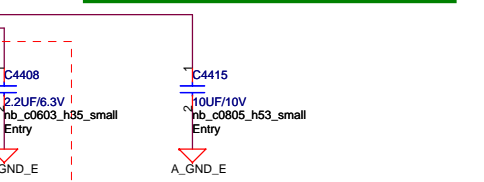
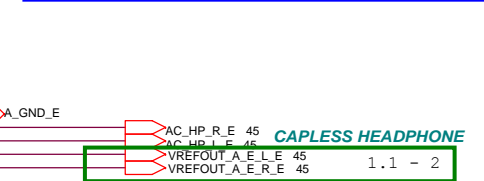
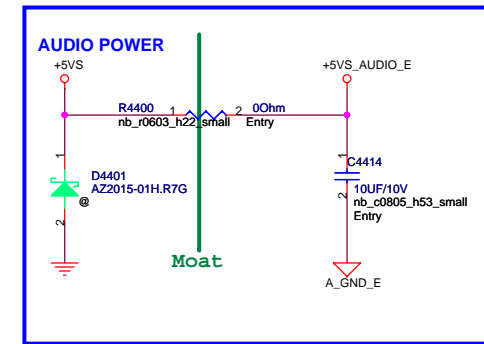
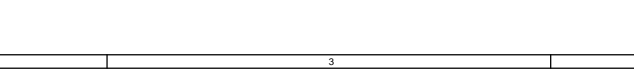
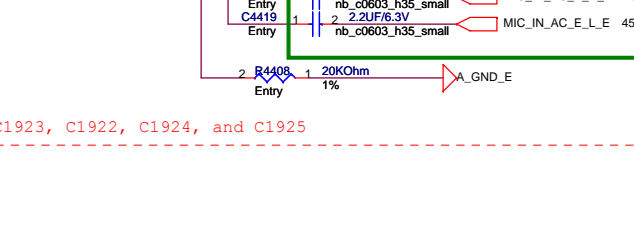
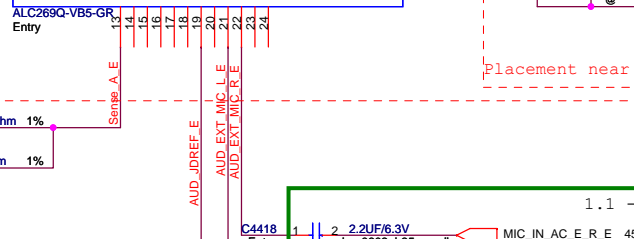
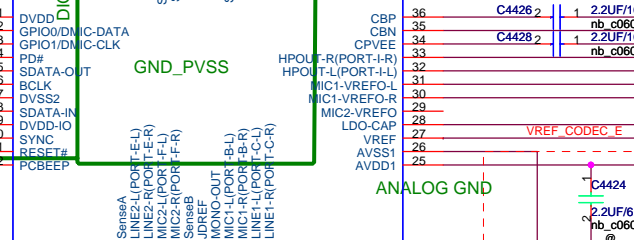
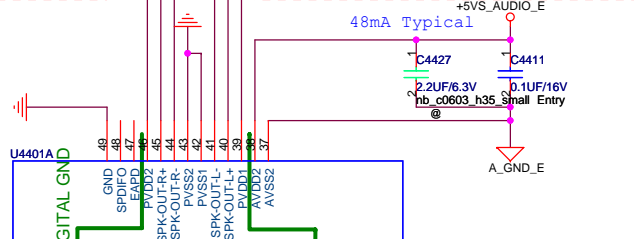
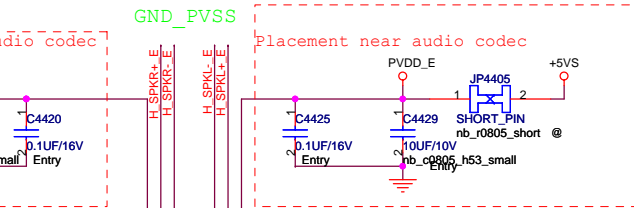
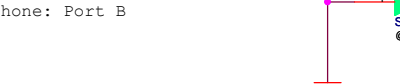
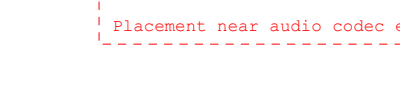
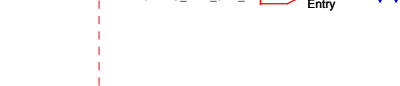
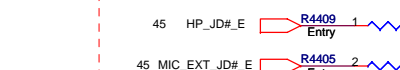
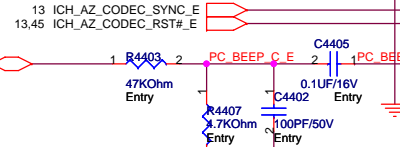
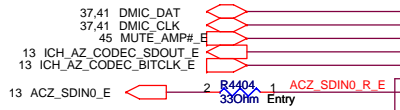
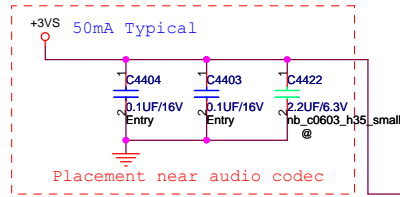
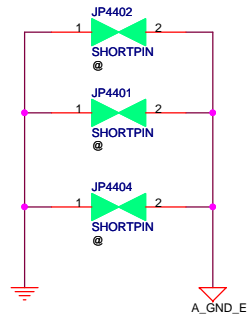


13,17,41 SPKR\_PCH

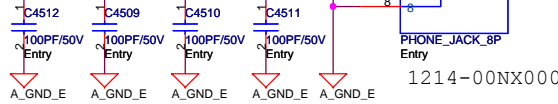
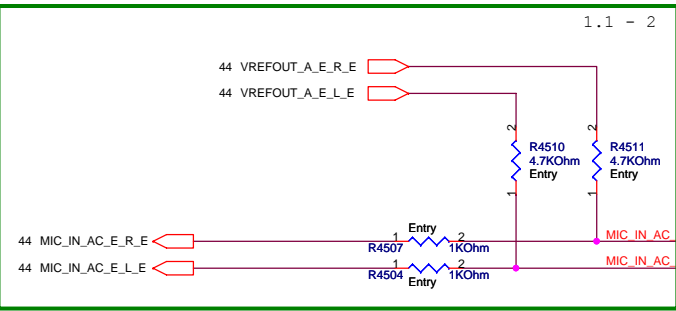
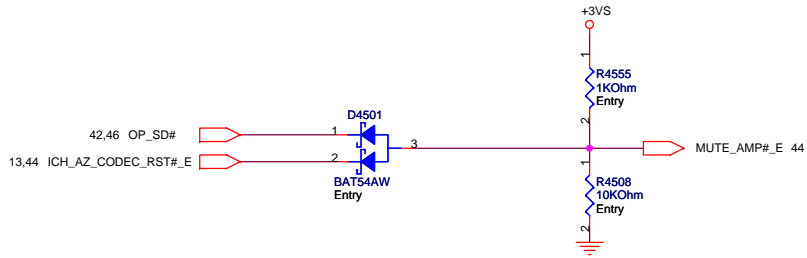


### Configuration for ALC269

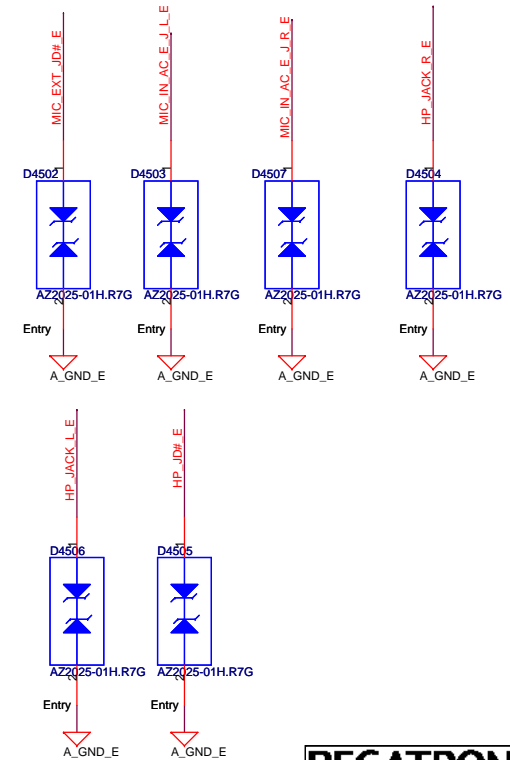
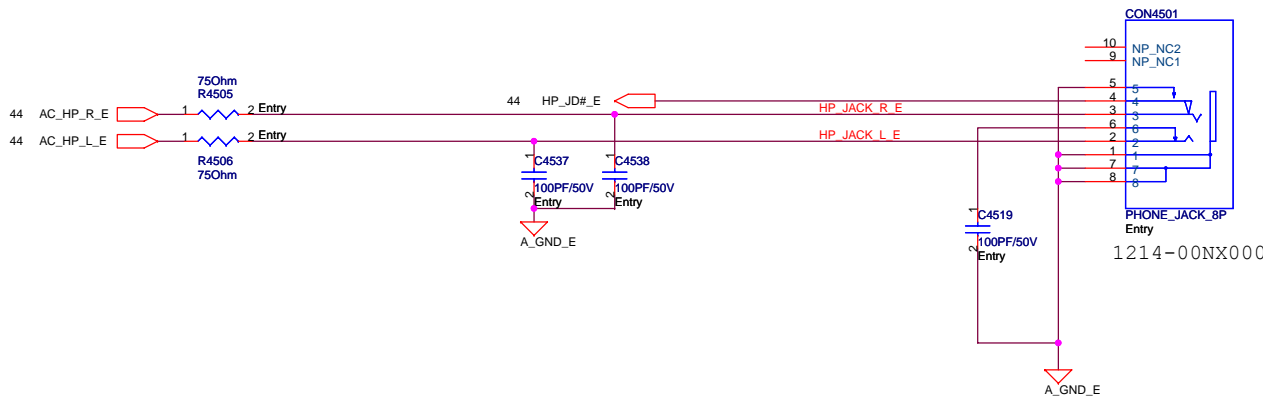
Internal Speaker: Port D  
External Headphone: Port A  
External Microphone: Port F  
Internal Microphone: Port B

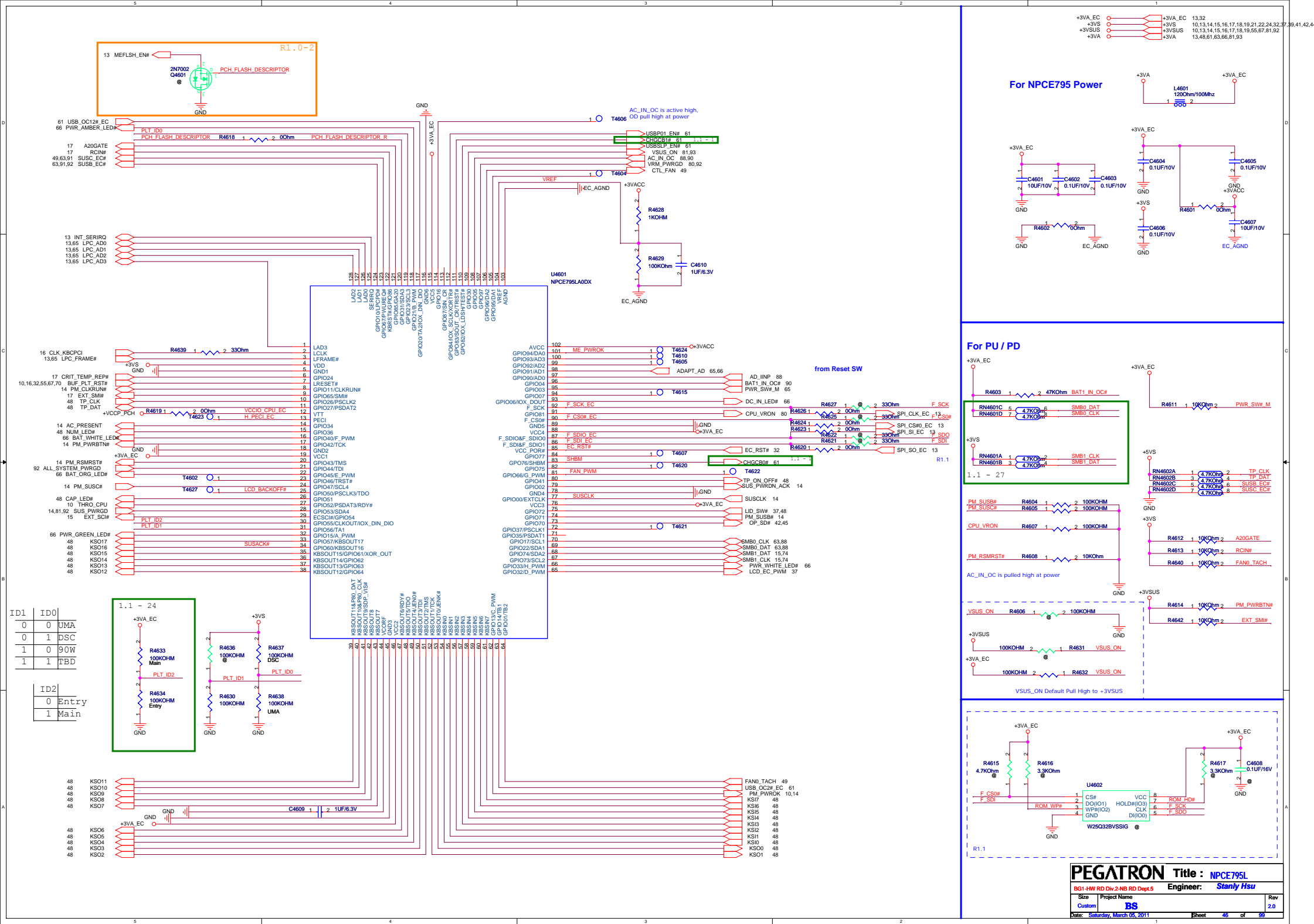


# AMP De-Pop Control circuit

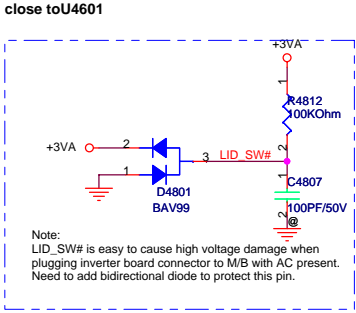
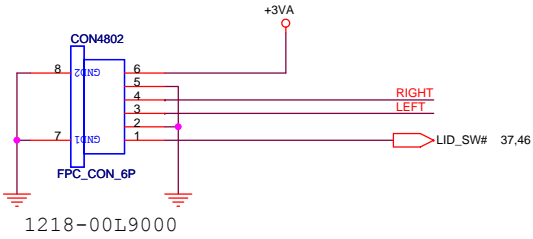


## HP JACK

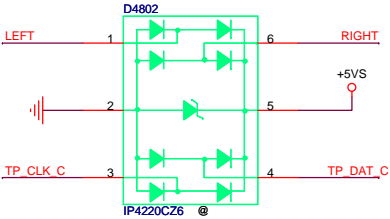
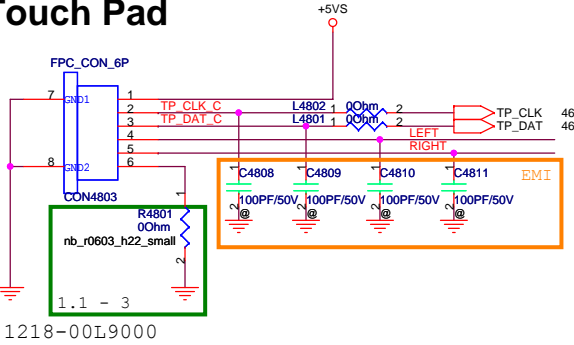




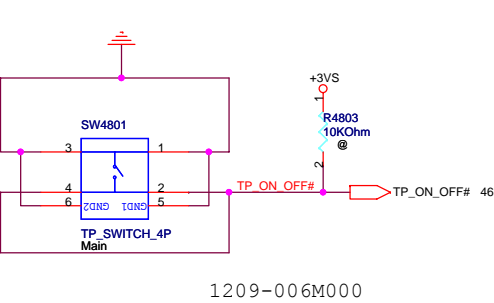
Touch Pad Button/ Hall Sensor



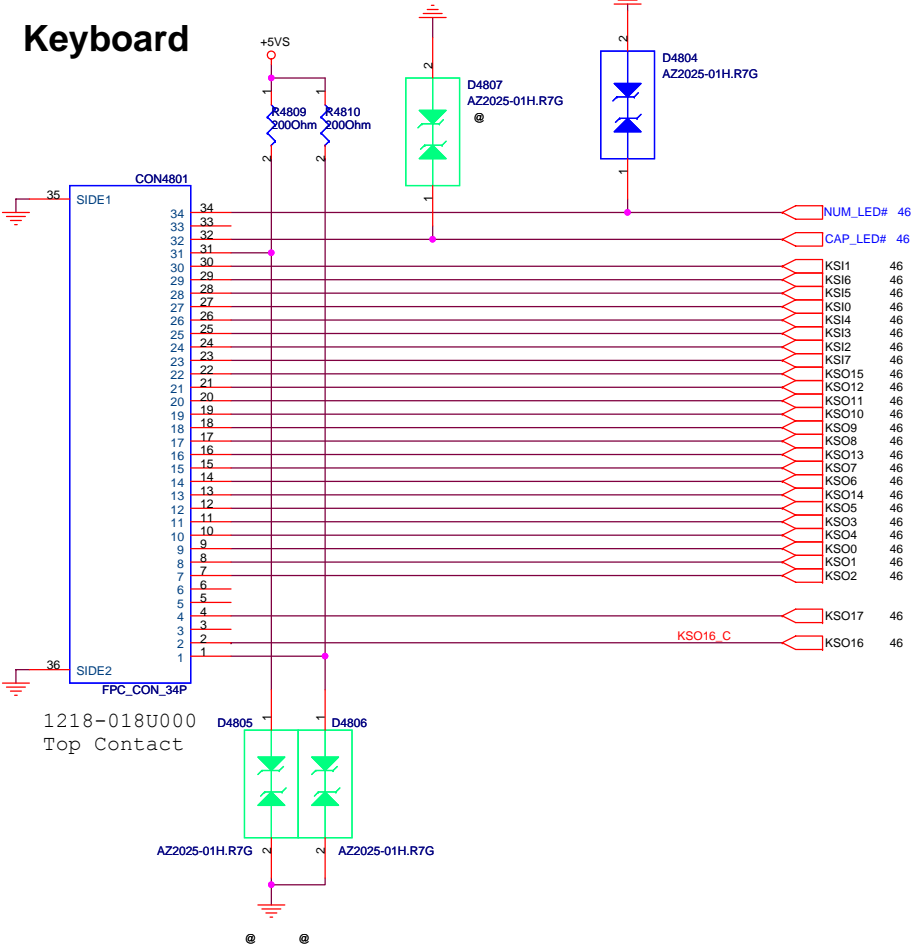
Touch Pad



TP On/Off



Keyboard



(3.6K: 92°C Protect  $\pm$  3%)

(3K: 94~ 99°C Protect)

RT4901  
10KOhm 3%  
MURATA/NCP15XH103E03RC

R4906  
100KOhm  
@

Q4901  
2N7002

SUSC\_EC# 46,63,91

FORCE\_OFF#\_EC 32

U4902  
NC2 VOUT  
VDD  
NC1 VSS  
IC-PST8213NR

C4904 2 0.1UF/16V

C4905 2 16V

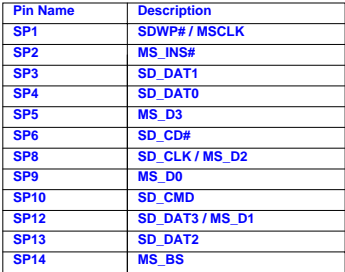
+5V

+5V

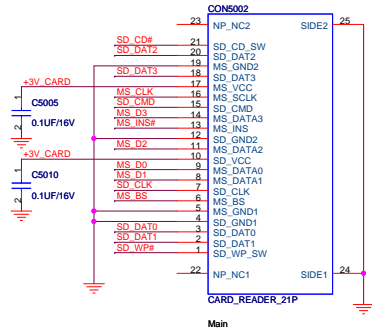
+5V

[illegible]

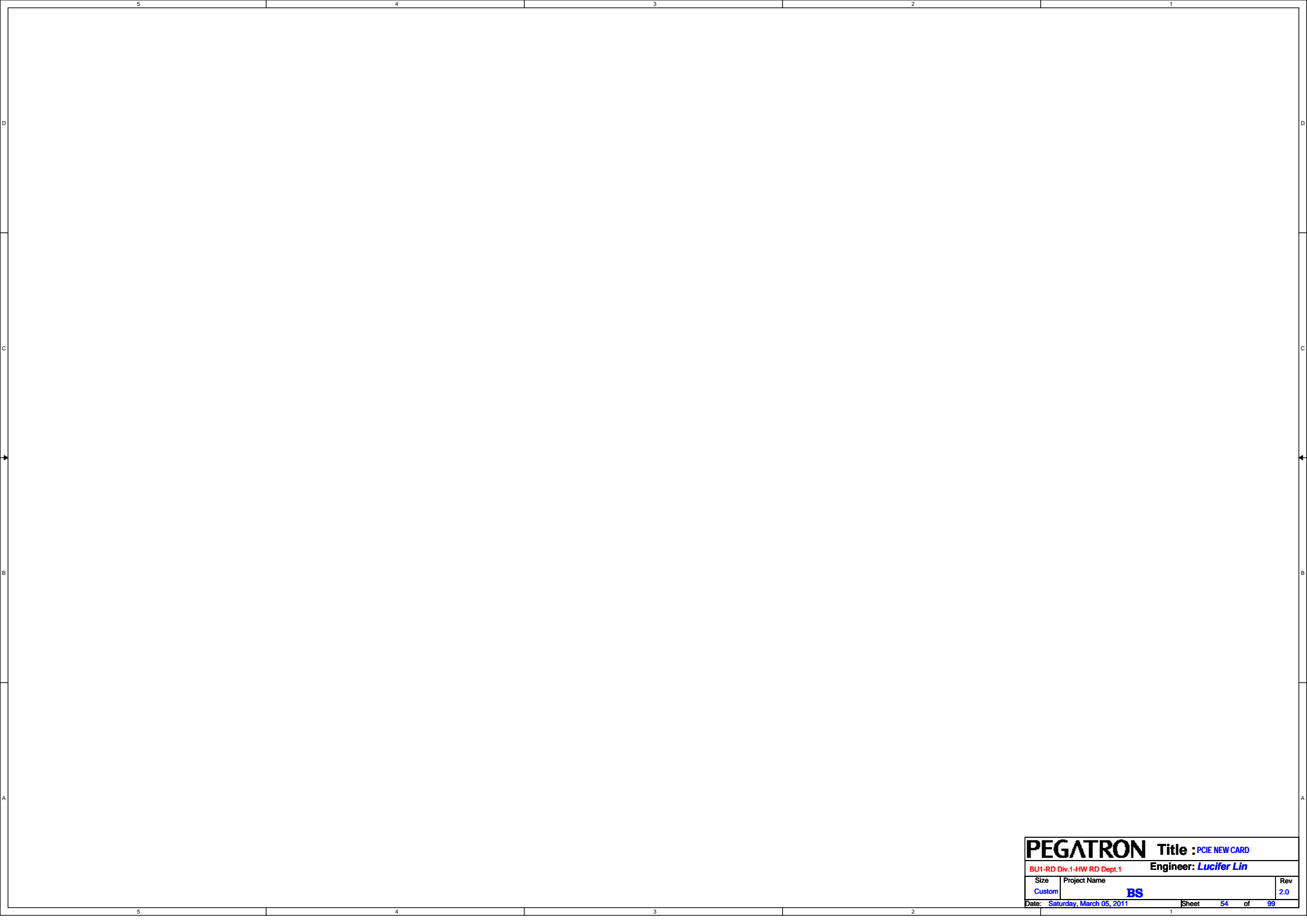


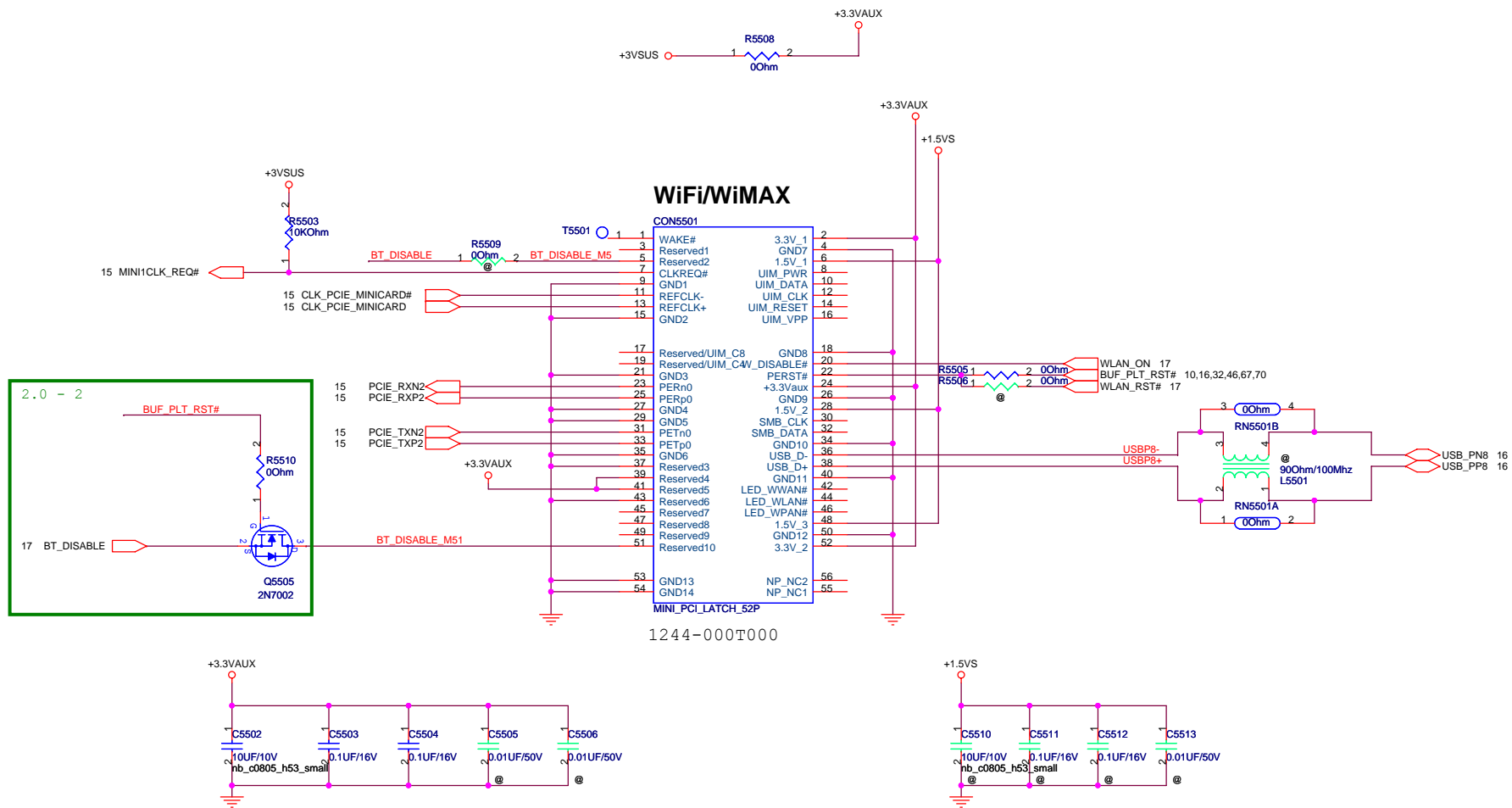


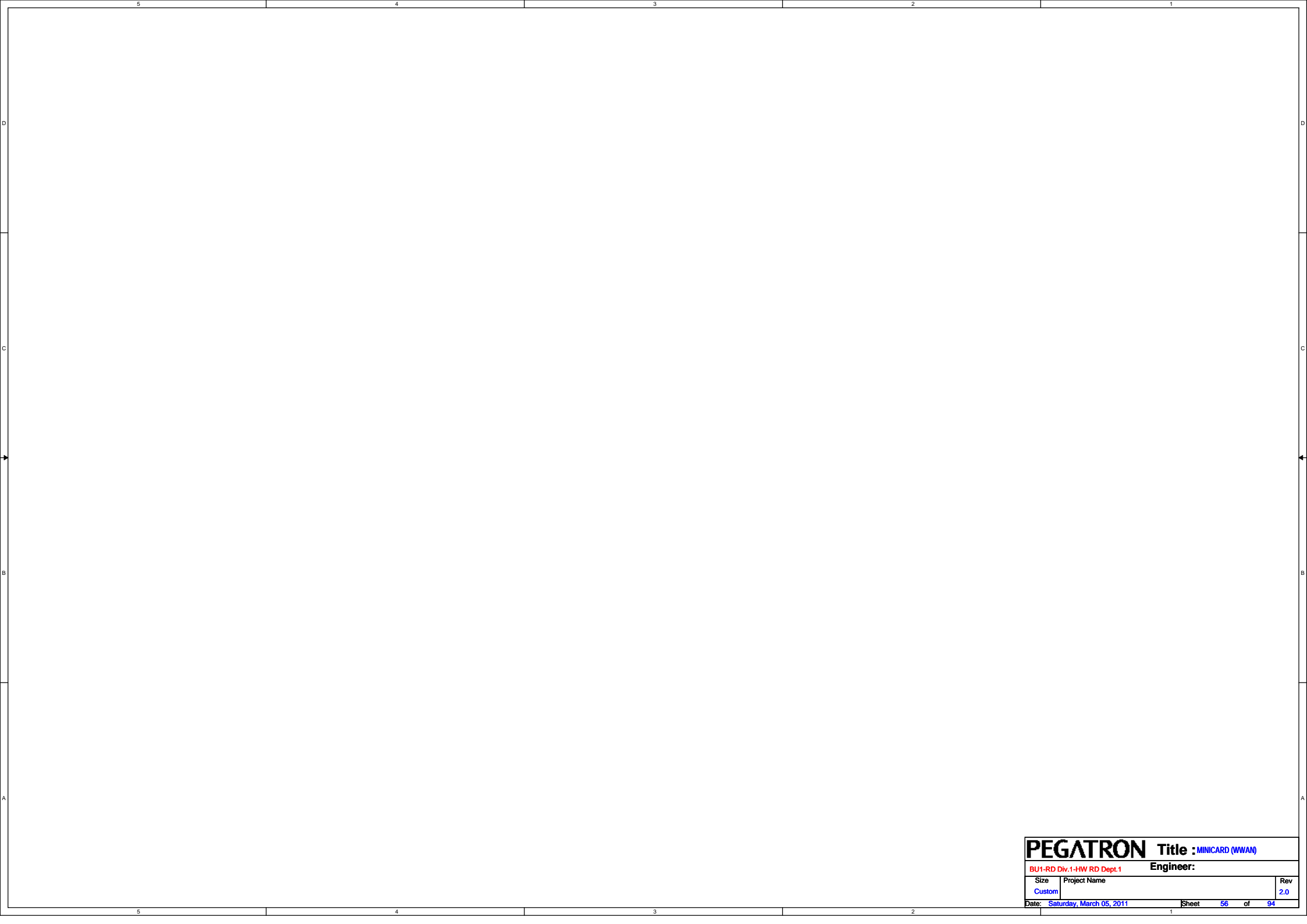
SP1	SD_WP#	MS_CLK
SP2		MS_IN#
SP3	SD_DAT1	
SP4	SD_DAT0	
SP5		MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9		MS_D0
SP10	SD_CMD	
SP12	SD_DAT3	MS_D1
SP13	SD_DAT2	
SP14		MS_BS





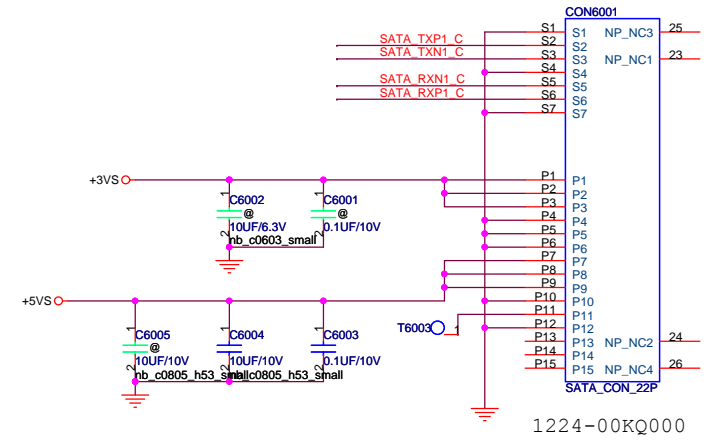
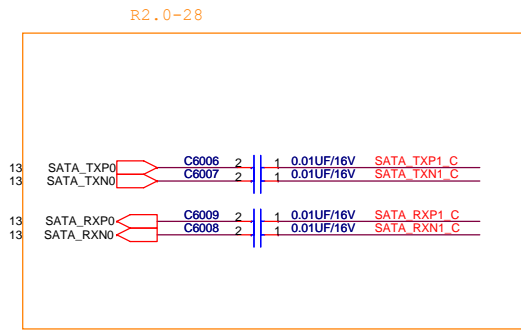






<b>PEGATRON</b>		<b>Title :</b> MINICARD (WWAN)	
BU1-RD Div.1-HW RD Dept.1		<b>Engineer:</b>	
Size	Project Name		Rev
Custom			2.0
Date: Saturday, March 05, 2011		Sheet	56 of 94

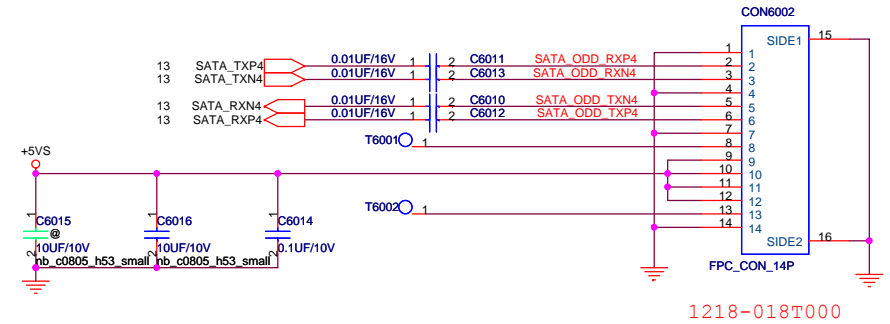




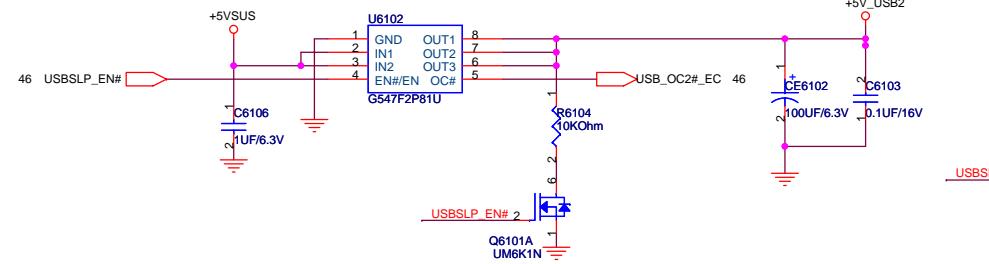
HDD

SSD

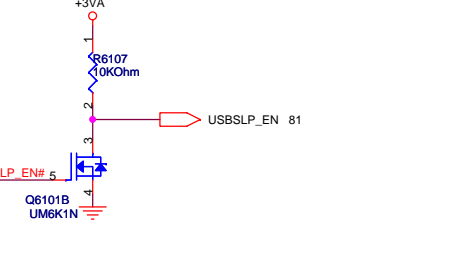
ODD



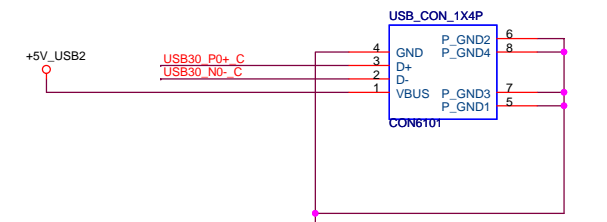
# USB 3.0/2.0/Sleep & Charge



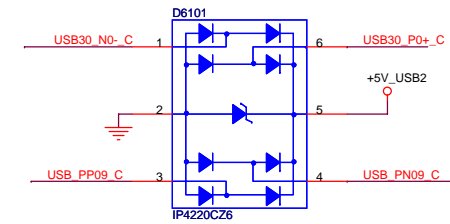
# USB PWR SWITCH



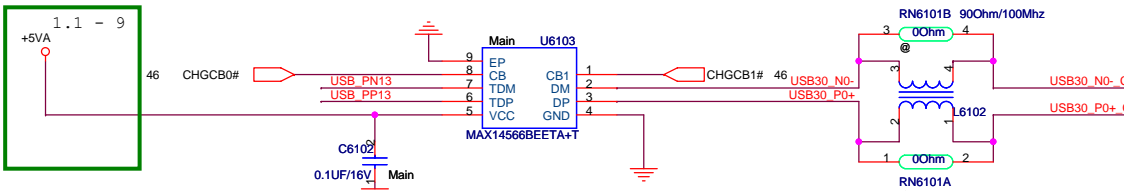
# USB 2.0



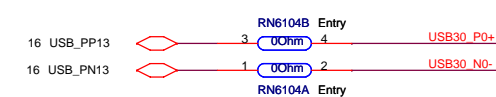
Main: 1213-00MN000  
Entry: 1213-00MN000



PLACE ESD Diodes 0700-0014000 near Connector



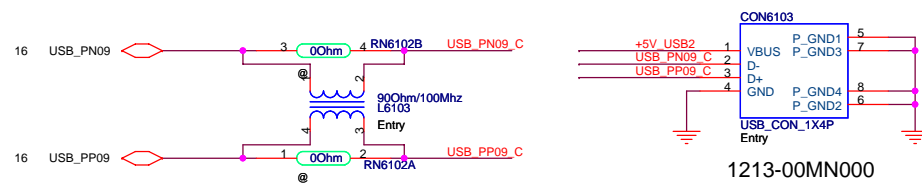
# Main/USB 2.0/w SLP&CHG



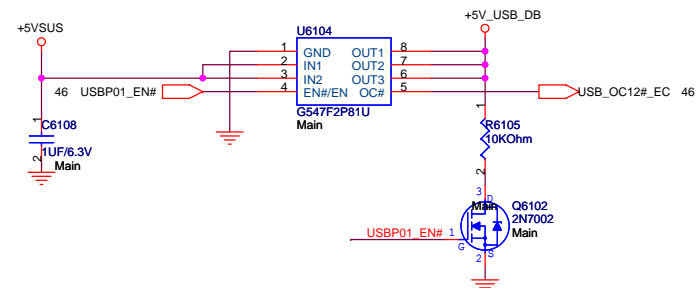
# Entry USB 2.0 Only

# USB Conn. for Entry colay HDMI

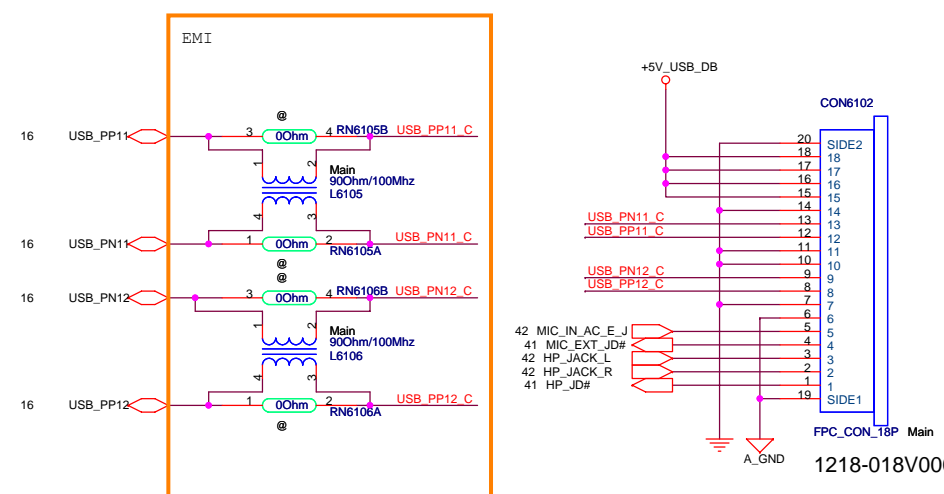
# USB 2.0



# USB Power Switch for USB DB Main



# AUDIO BOARD/w USB2.0 x2





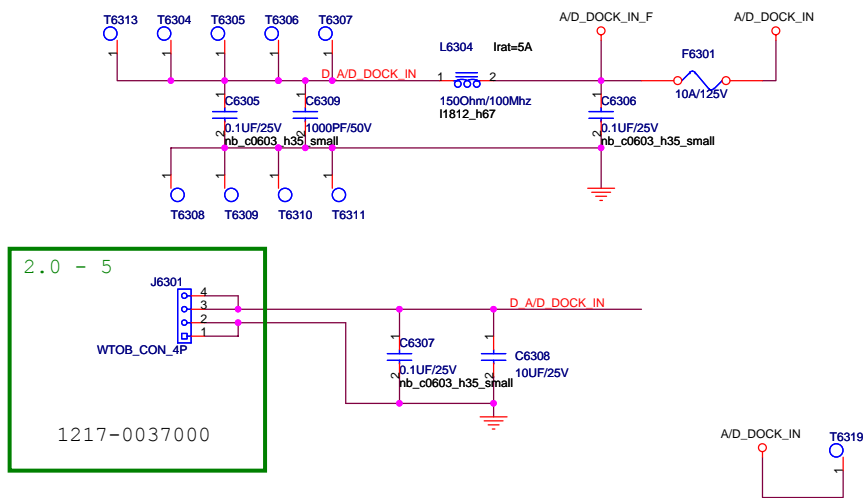
TouchPanel CON

Camera Module CON

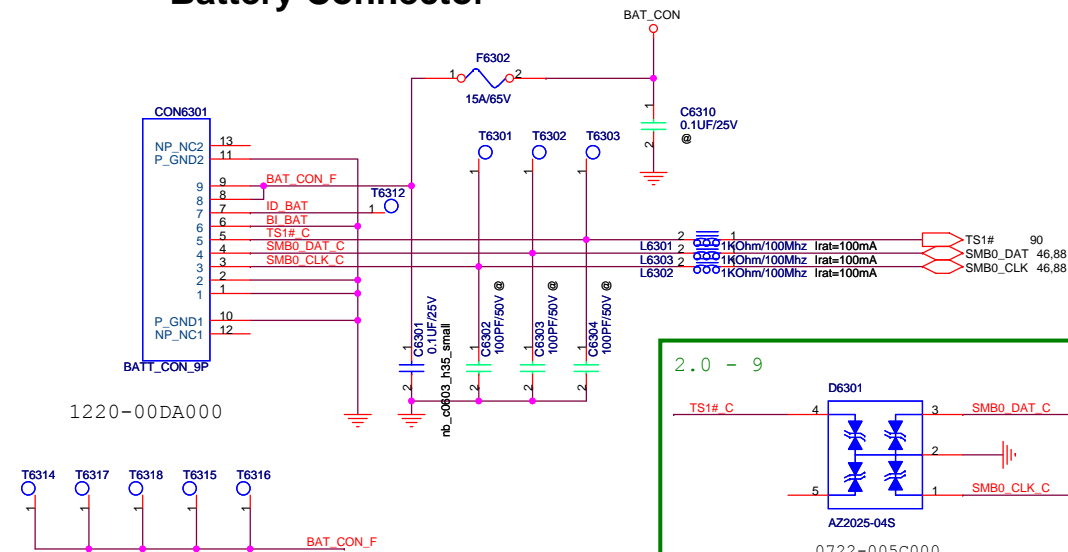
B/T MODULE

FELICA MODULE

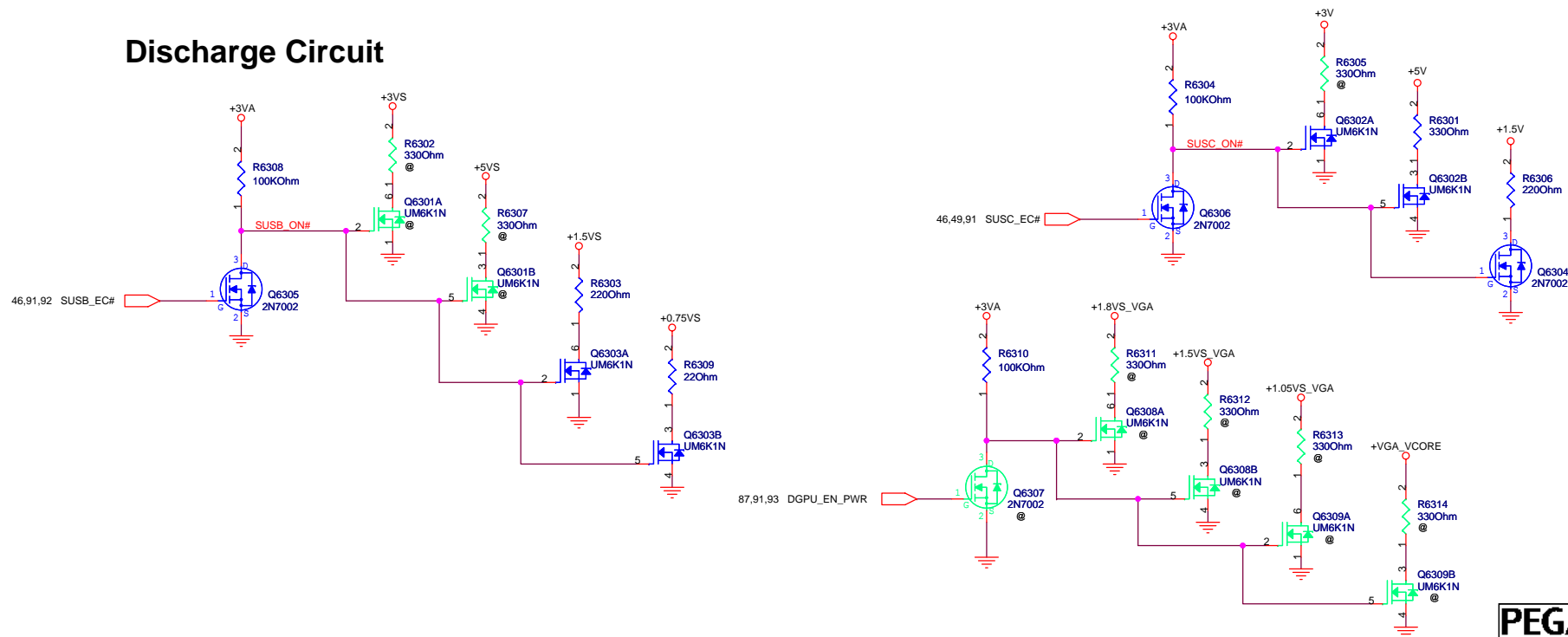
## DC IN



## Battery Connector



## Discharge Circuit



**PEGATRON** Title : DC-IN/ DISCHARGE

BU1-RD Div.1-HW RD Dept.1

Engineer: **ChingPo Chen**

Size Project Name

Custom

**BS**

Rev

2.0

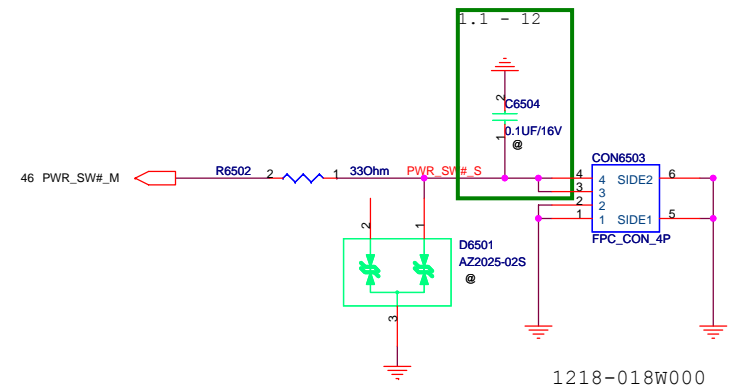
Date: Saturday, March 05, 2011

Sheet 63 of 99



Notes:  
BRAIDWOOD right angled Connector (1.8V keyed)  
Compatible BRAIDWOOD Modules  
1.8V Mobile NVM 4GB 31.60mm x21.5mm  
1.8V Mobile NVM 8GB 31.60mm x 21.5mm  
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

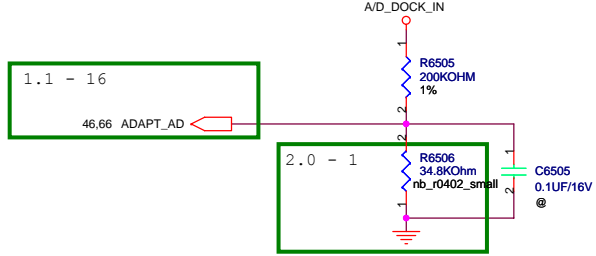
PWR BRD/ AMBIENT/ HALL CONN.



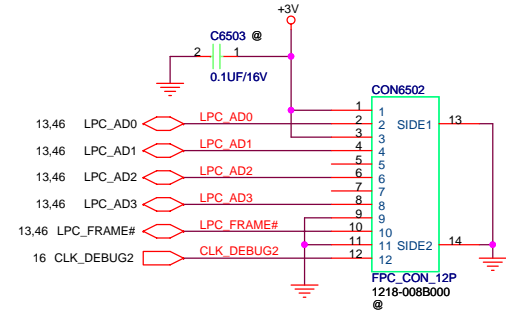
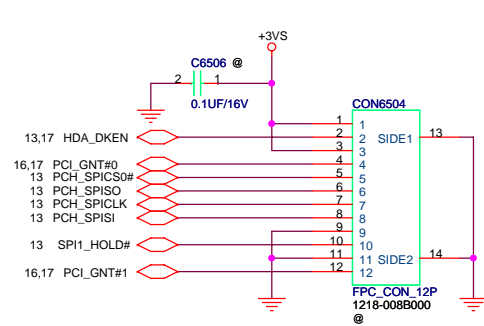
MODEM MODULE

KILL SWITCH.

ADAPTOR VOLTAGE DETECTOR.



DEBUG CARD CONN.



# LED (Main)

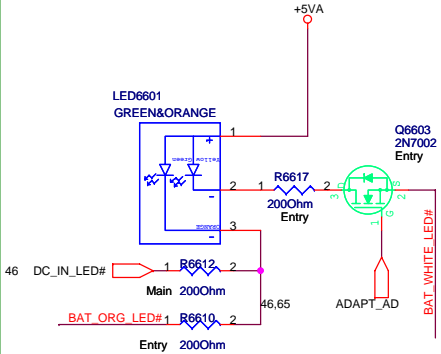
Left → Right

**DC-IN** **Power** **Main Battery** **HDD/ODD** **Bridge Media** **WiFi**

White White White White White White  
Amber (Blink) Amber (Blink)

1.1 - 7  
1.1 - 26

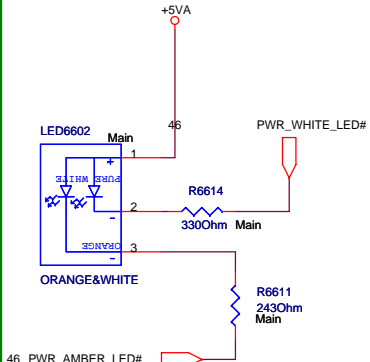
## Main: DC IN Entry: DC IN/BATT CHRG



Main / White 0713-006F000  
Entry / Duel 0713-00W4000 G/A

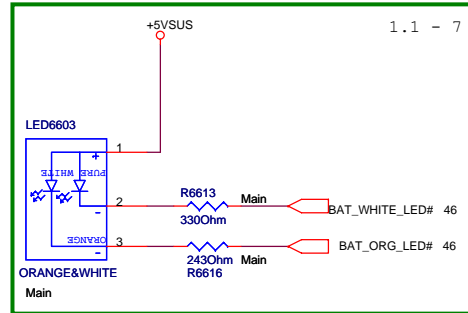
1.1 - 13  
1.1 - 25

## Power LED



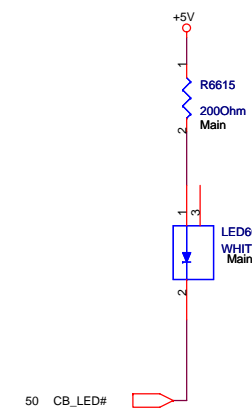
Main / Duel 0713-001P000

## Battery

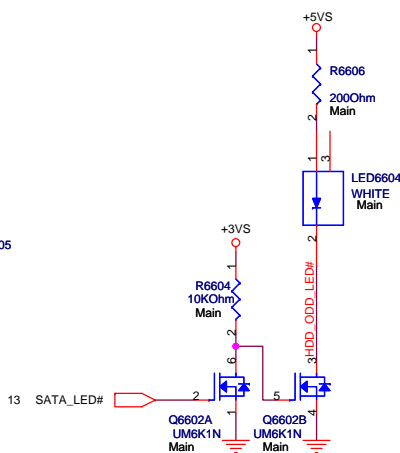


1.1 - 7

## Bridge Media

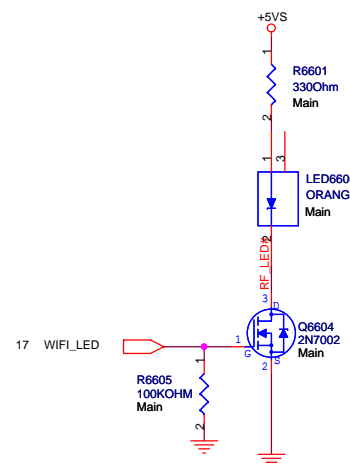


## HDD/ODD



## Connectivity(WLAN/WiMAX)

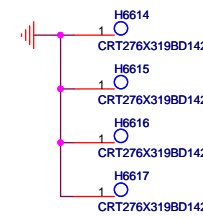
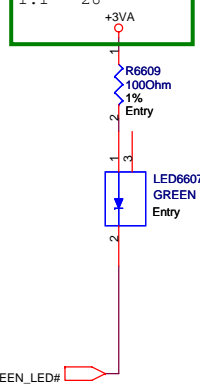
Main / Amber 0713-0046000



## LED (Entry)

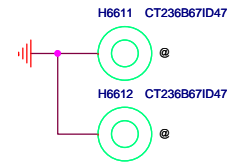
### Power LED

1.1 - 7  
1.1 - 28

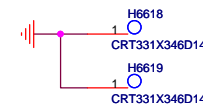


Screw Px4  
CPU

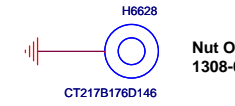
PCH Local Side Symbol



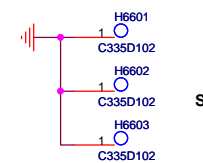
PCH Nut x2  
1308-005J000



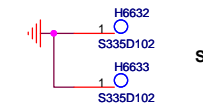
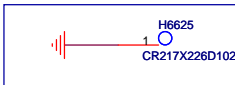
Screw Dx2  
VGA



Nut Ox1 (MINICARD)  
1308-007D000

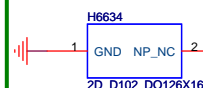
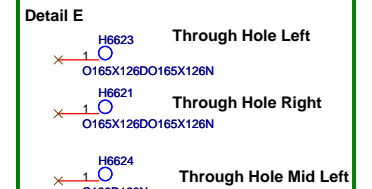


Screw Gx3



Screw Ax2

1.1 - 18

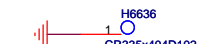


Screw Hx1

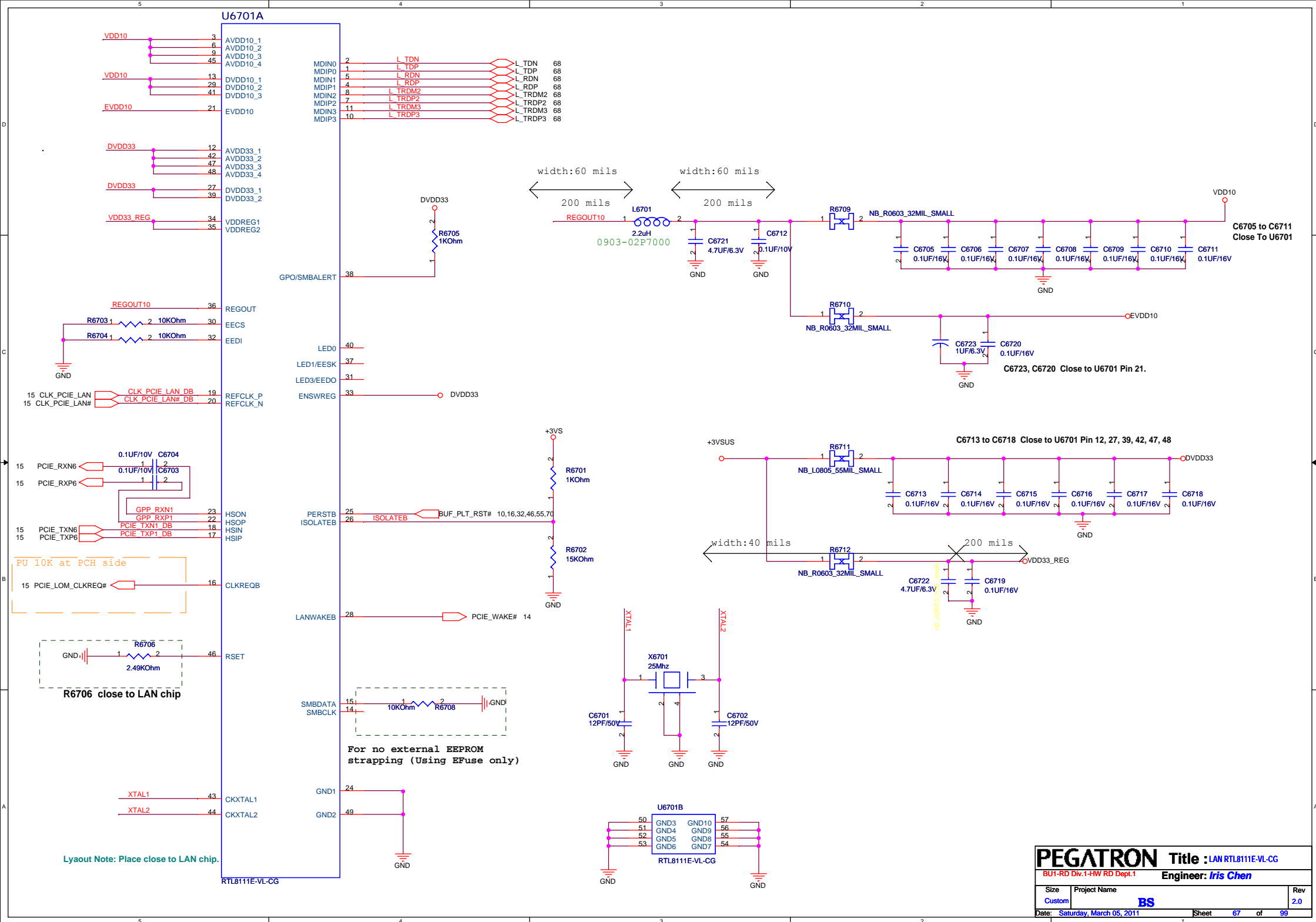
1.1 - 20



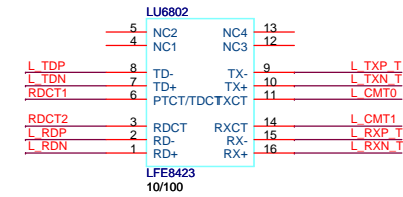
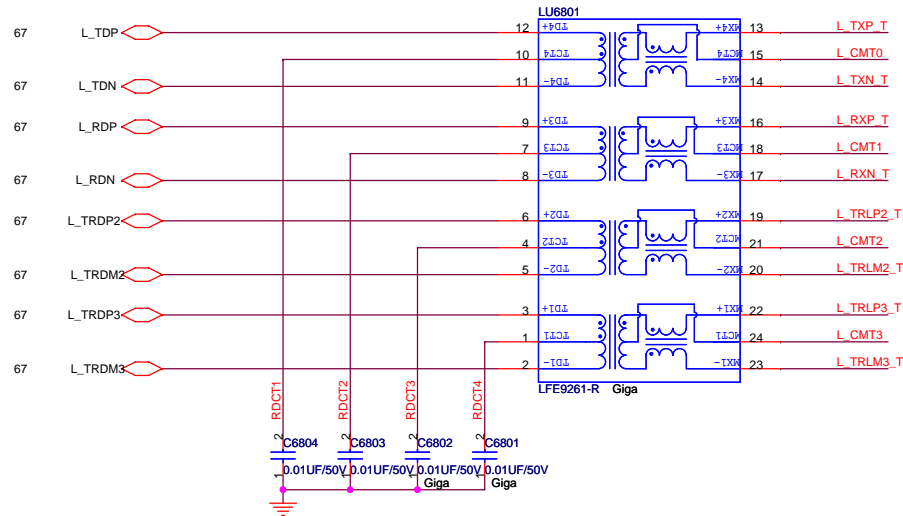
Screw Kx2



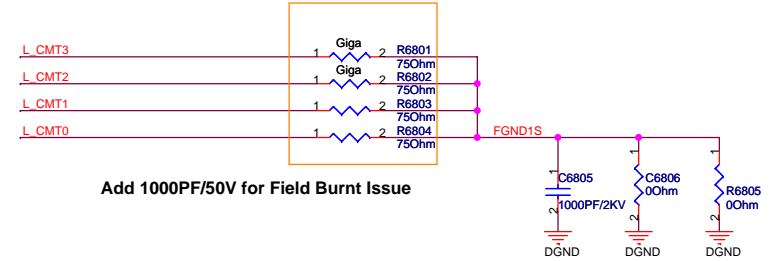
Screw Lx1



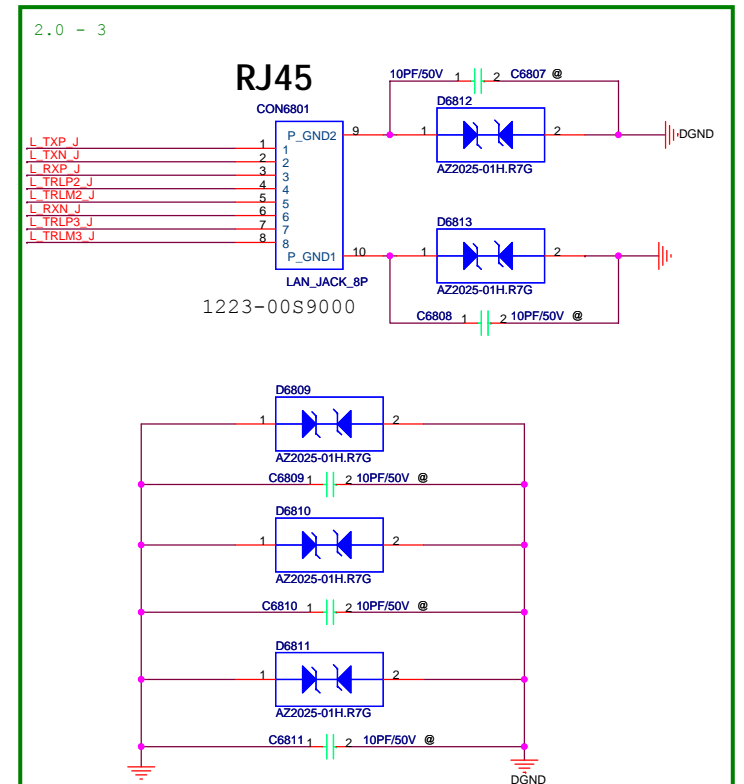
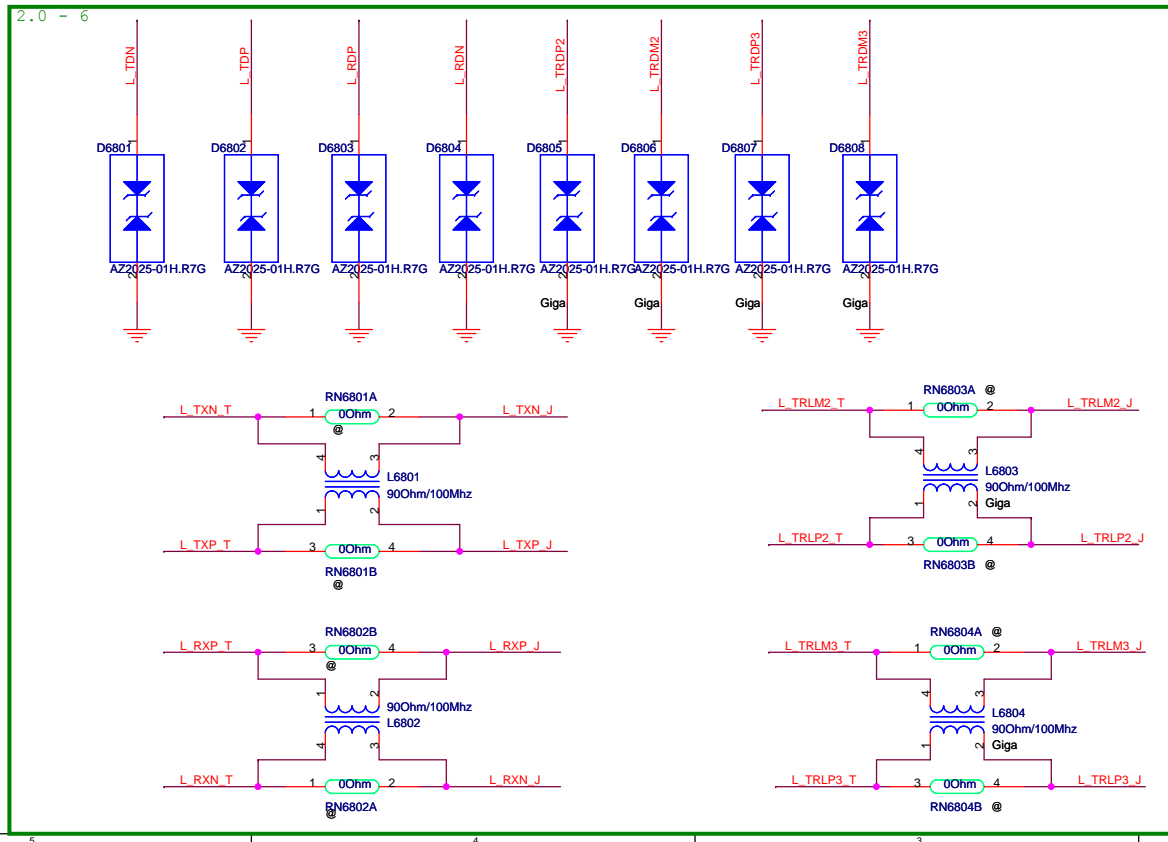
# Co-Layout

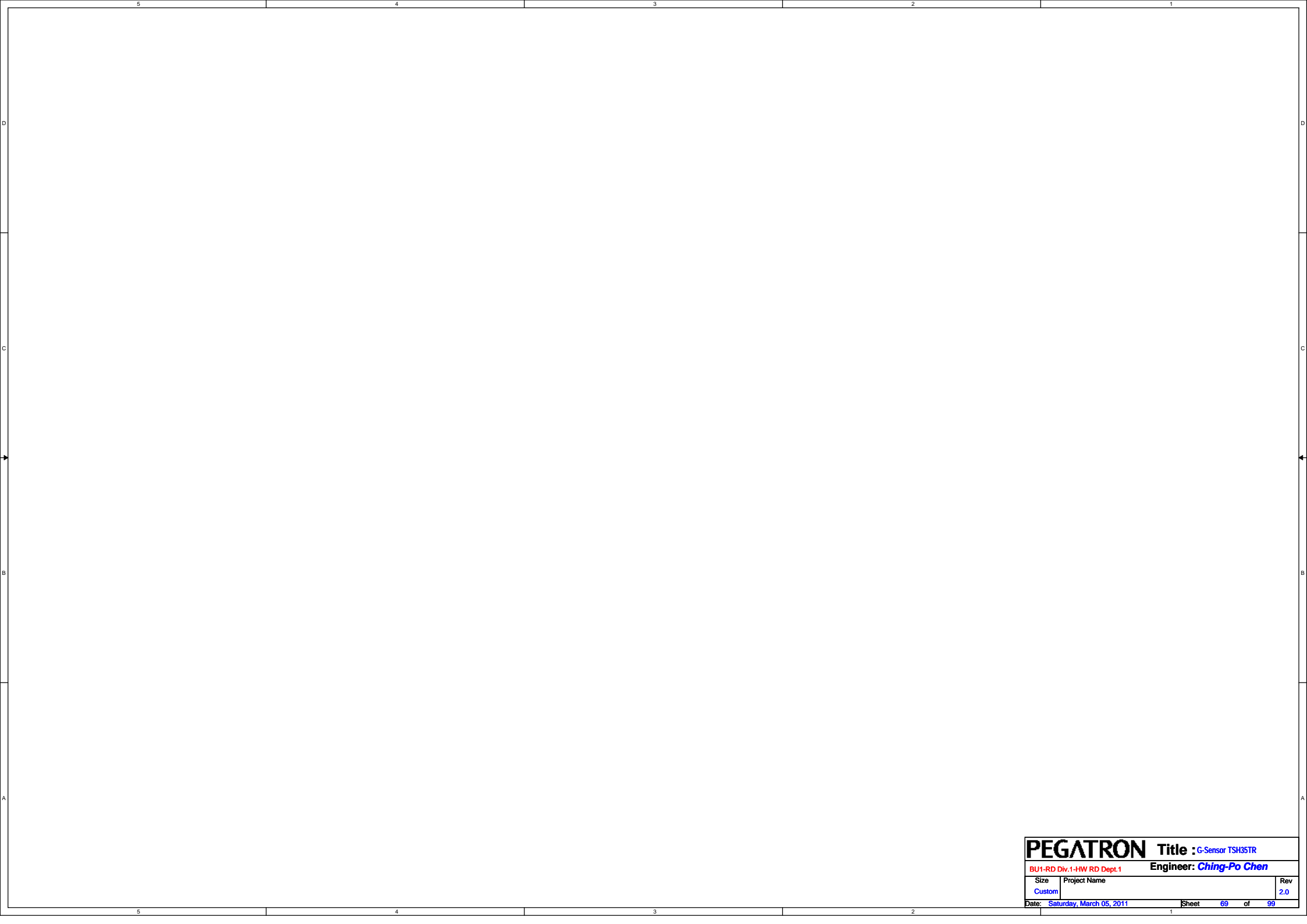


Change LRN301 to LR305, LR306, LR307 and LR308 for Layout Placement

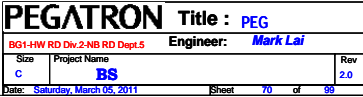


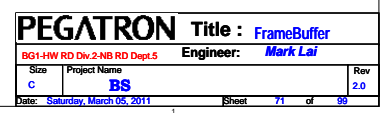
Add 1000PF/50V for Field Burnt Issue

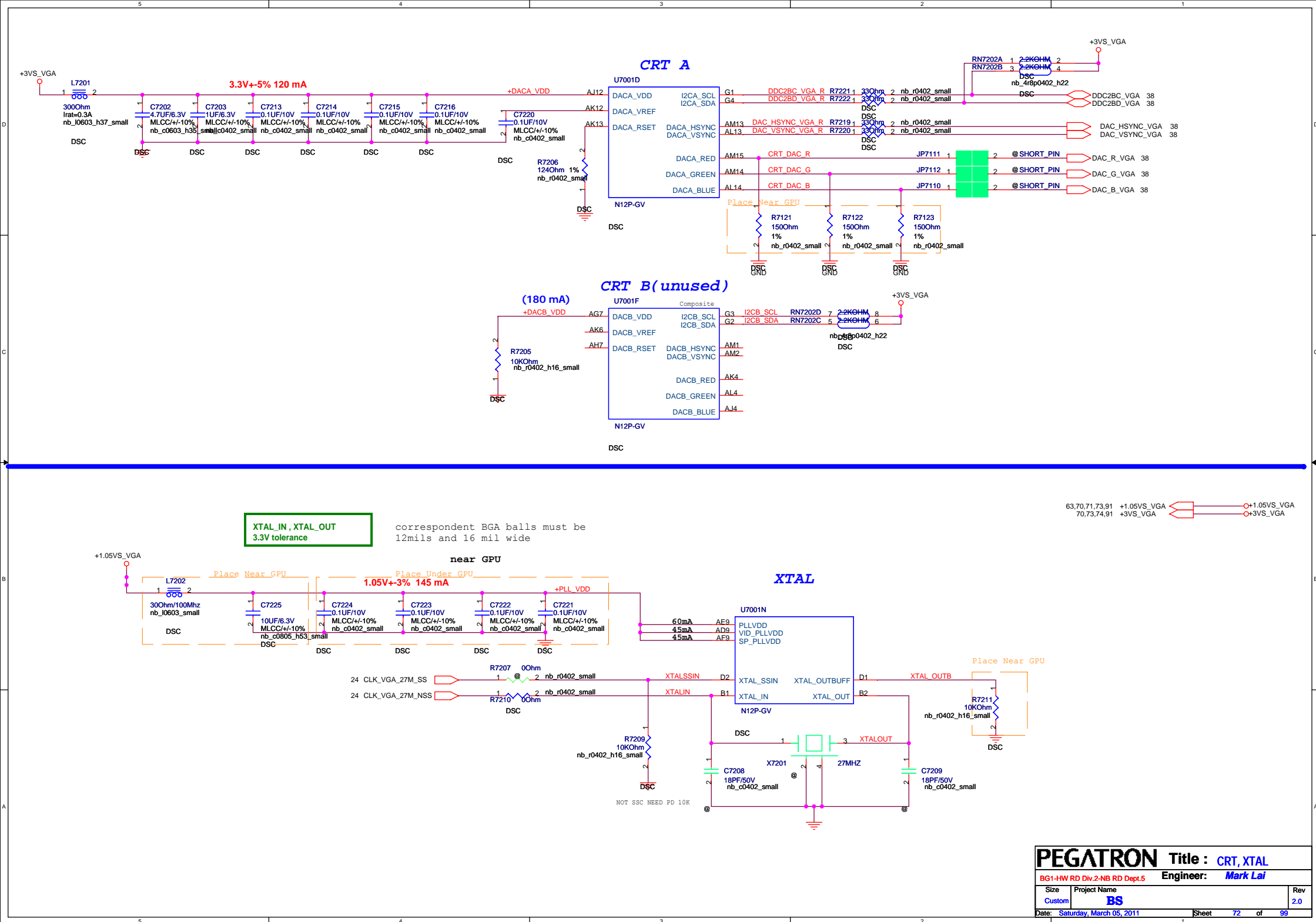




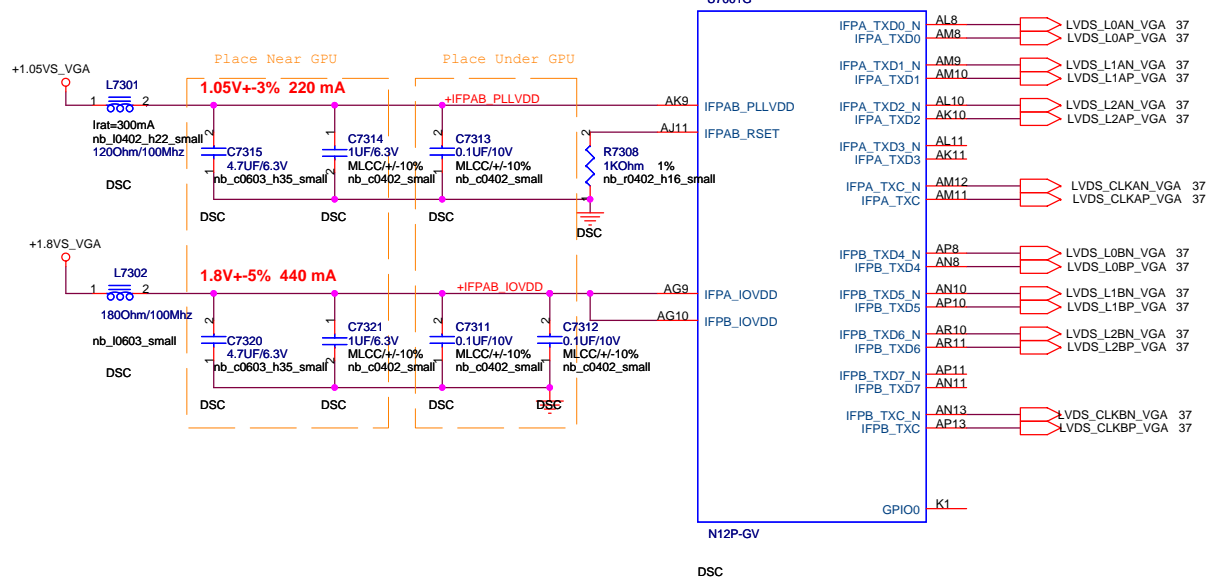




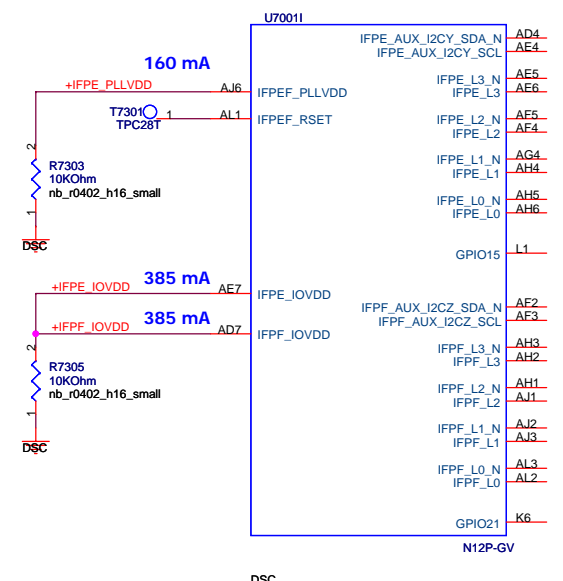




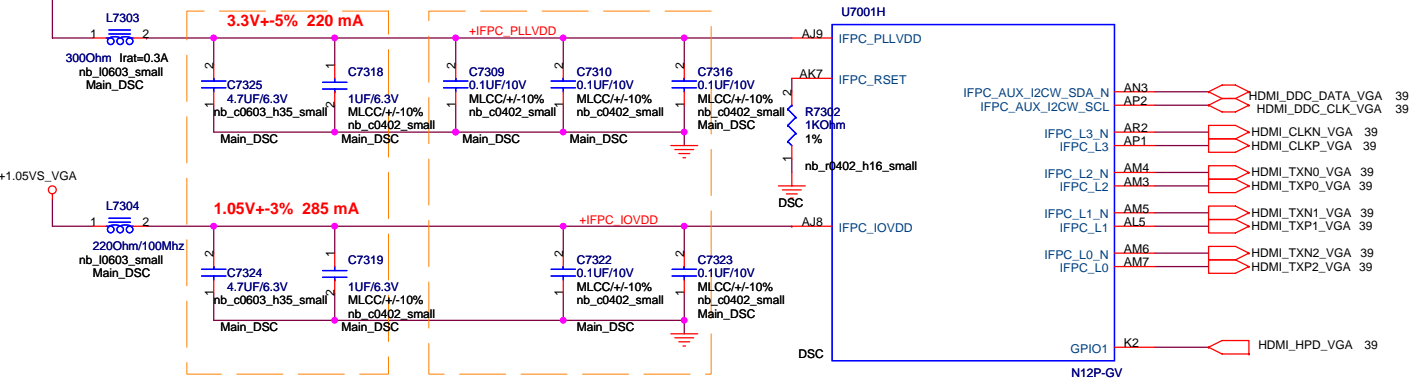
## LVDS (LINK A & B)



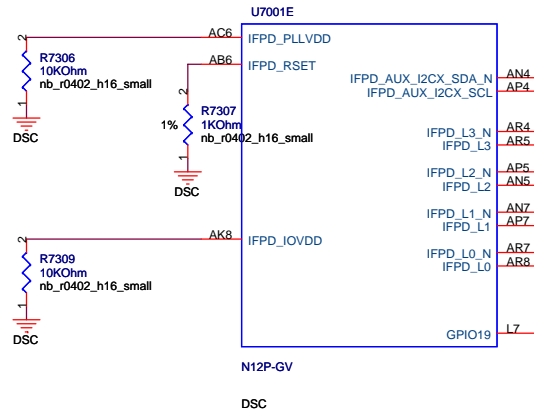
## DP unused (LINK E & F)



## HDMI (LINK C)



## DP unused (LINK D)



IFPx	A	B	C	D	E	F
TURKEY	LVDS A	LVDS B	HDMI	unused		

63,70,71,72,91 +1.05VS\_VGA

63,91 +1.8VS\_VGA

70,72,74,91 +3VS\_VGA

**PEGATRON** Title : LVDS, HDMI

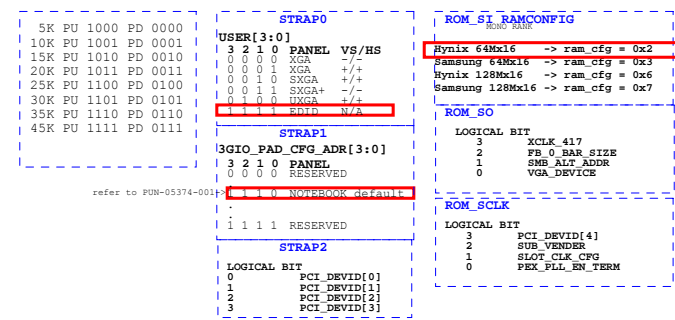
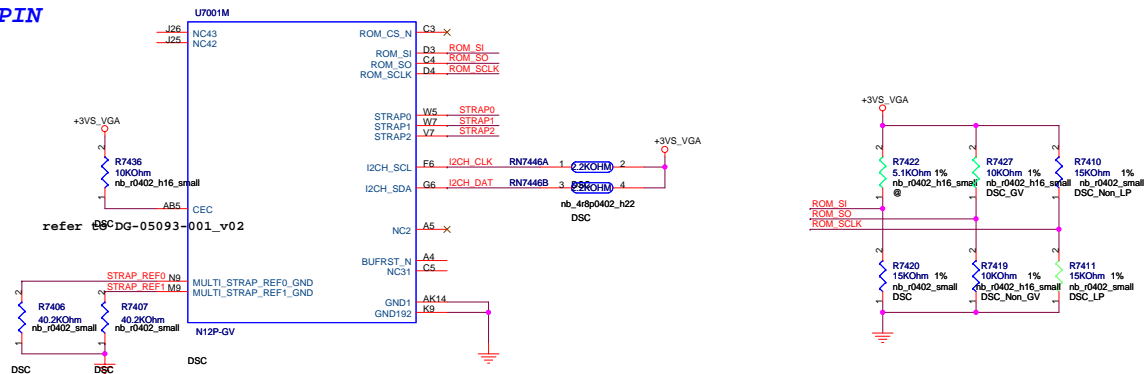
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Mark Lai

Size Project Name

Custom BS

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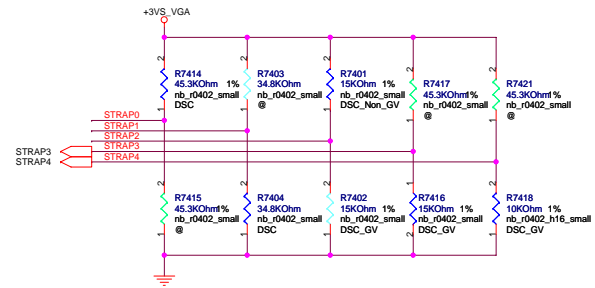
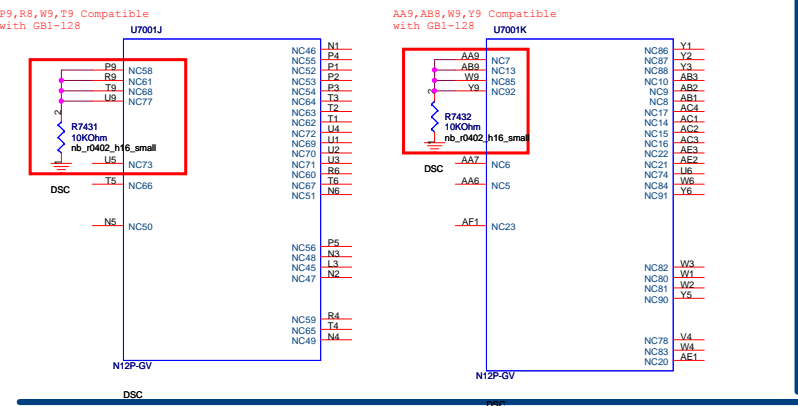
## STRAP PIN



refer to PUN-05374-0012

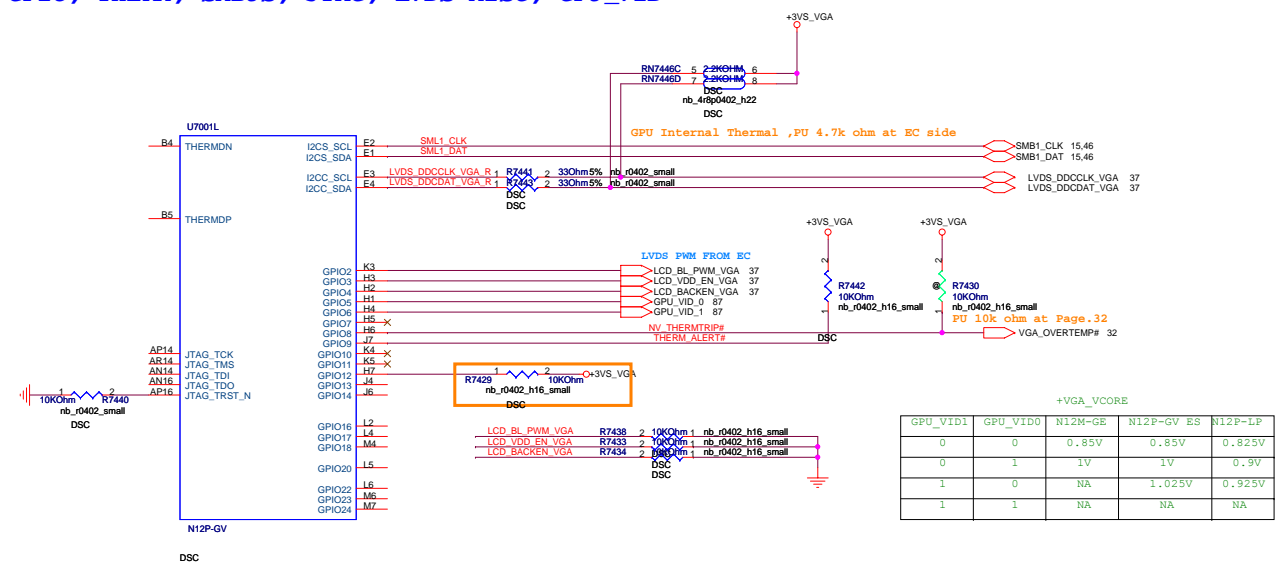
70.72.73.91 +3VS\_VGA

## Muti I/O unused



			N12P-LP QS		N12P-GV ES		N12M-GE QS	
			PU	PD	PU	PD	PU	PD
ROM_SO	R7427	R7419	@	10K	@	10K	@	10K
ROM_SCLK	R7410	R7411	@	15K	15K	@	15K	@
ROM_SI	R7422	R7420	@	H 64:15K \$ 64:20K	@	H 64:15K \$ 64:20K	@	H 64:15K \$ 64:20K
Strap2	R7401	R7402	25K	@	45K	@	15K	@
Strap1	R7403	R7404	@	35K	@	35K	@	35K
Strap0	R7414	R7415	45K	@	45K	@	45K	@
Strap3	R7417	R7416	@	@	@	20k	@	@
Strap4	R7421	R7418	@	@	@	10k	@	@

## GPIO, THERM, SMBUS, JTAG, LVDS MISC, GPU\_VID



GPU_VID1	GPU_VID0	N12M-GE	N12P-GV ES	N12P-LP
0	0	0.85V	0.85V	0.825V
0	1	1V	1V	0.9V
1	0	NA	1.025V	0.925V
1	1	NA	NA	NA

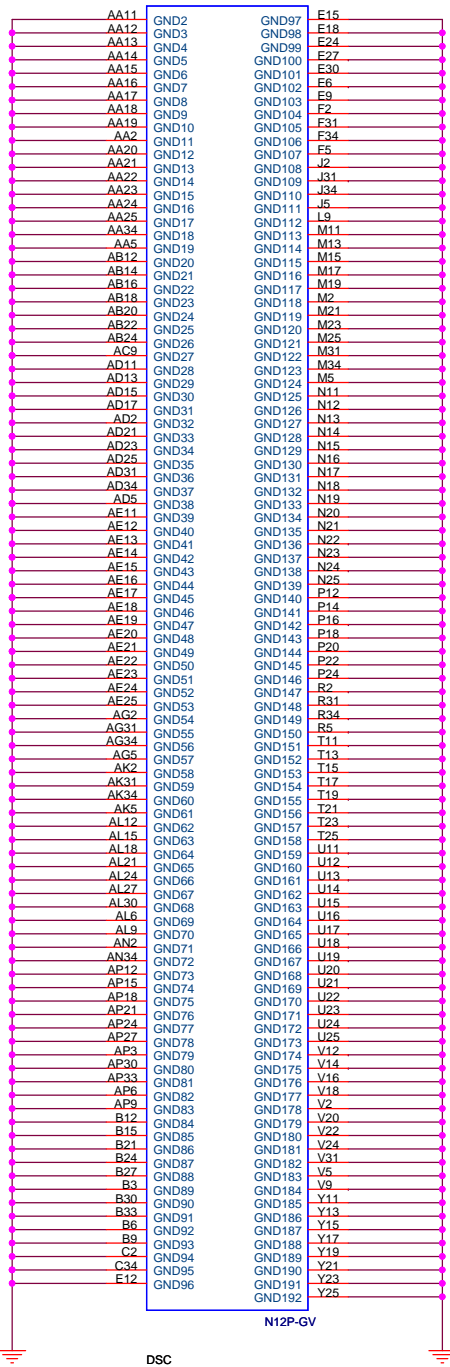
Table 12.1 GPIO Description

GPIO PIN Name	Normal Function	I/O	Functional Description
GPIO0	General Purpose		
GPIO1	HPD_C	I	Hot Plug Detect for IFPC
GPIO2	LCD0_BL_PWM	O	Panel Backlight Brightness Control (PWM capable)
GPIO3	LCD0_VCC	O	Panel Power/Enable
GPIO4	LCD0_BLEH	O	Panel Backlight ON/OFF Control (PWM capable)
GPIO5	GPU_VID0	O	GPU Core VDD VID0
GPIO6	GPU_VID1	O	GPU Core VDD VID1
GPIO7	GPU_VID2	O	GPU Core VDD VID2
GPIO8	OVERT	I/O	Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	SLI_RASTER_SYNC	I/O	SLI Raster Sync
GPIO12	PWR_LEVEL	I	AC Power Detect Input
GPIO13	THERM_LOAD_STEP_DOWN	O	Power Supply Control
GPIO14	THERM_LOAD_STEP_UP	O	Power Supply Control
GPIO15	HPD_E	I	Hot Plug Detect for IFPE
GPIO16	FAH_PWM	O	Programmable Fan Control
GPIO17	Reserved		
GPIO18	Reserved		
GPIO19	HPD_D	I	Hot Plug Detect for IFPD
GPIO20	Reserved		
GPIO21	HPD_F	I	Hot Plug Detect for IFPF
GPIO22	SWAPRDY	I	SLI Swap Ready Signal
GPIO23	3Dvision	O	3Dvision functions
GPIO24	General Purpose		

PEGATRON Title: STRAP,THERM,ROM,MMIO

GND

U7001O

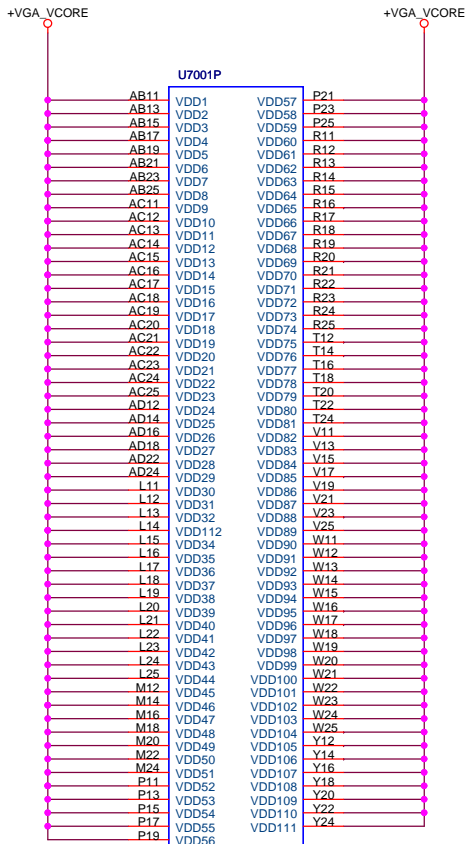


DSC

N12P-GV

VAG\_VCORE

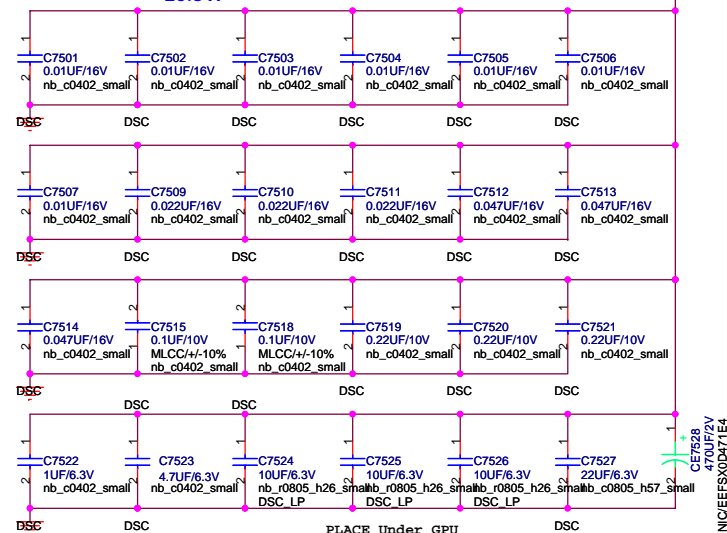
U7001P



N12P-GV

DSC

20.3 A



63.87 +VGA\_VCORE



**\*TOP SIDE\***

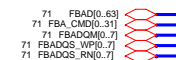


Table 5.4 Mode E Command Mapping

#12x Fermi DDR3 mode E	Data Bits [31:0]	Data Bits [63:32]
FBX_CMD0	ODT	
FBX_CMD1	C51*	
FBX_CMD2	C50*	
FBX_CMD3	CKE	
FBX_CMD4	A9	A11
FBX_CMD5	A6	A7
FBX_CMD6	A3	BA1
FBX_CMD7	A0	A12
FBX_CMD8	A8	AB
FBX_CMD9	A12	A0
FBX_CMD10	A1	A2
FBX_CMD11	RS*	RS*
FBX_CMD12	A13	A14
FBX_CMD13	BA1	A3
FBX_CMD14	A14	A13
FBX_CMD15	CAS*	CAS*
FBX_CMD16	CKE	CKE
FBX_CMD17	C51*	C51*
FBX_CMD18		C50*
FBX_CMD19		ODT
FBX_CMD20	RST	RST
FBX_CMD21	A7	A6
FBX_CMD22	A4	A5
FBX_CMD23	A11	A9
FBX_CMD24	A2	A1
FBX_CMD25	A10	WE*
FBX_CMD26	A5	A4
FBX_CMD27	BA2	A15
FBX_CMD28	WE*	A10
FBX_CMD29	BA0	BA0
FBX_CMD30	A15	BA2
FBX_CMD31		







+3VS_VGA	<b>490 mA</b>	
	70 PEG	
	70 PEG	3.3V+5% 150 mA
	72 CRT, XTAL	3.3V+5% 120 mA
+1.05VS_VGA	<b>3.205A</b>	
	70 PEG	1.05V+3% 2200 mA
	70 PEG	1.05V+3% 120 mA
	72 CRT, XTAL	1.05V+3% 145 mA
+VGA_VCORE	<b>21.2A</b>	
	75 GPU PWR/GND	TBD
	77 78 FrameBuffer A&B	1.5V+5% / 5.2A
	71 FrameBuffer	1.5V+5% / 3.4A
+1.5VS_VGA	<b>8.6A</b>	
	73 LVDS, HDMI	1.8V+5% / 440 mA
+1.8VS_VGA	<b>440mA</b>	
	73 LVDS, HDMI	1.8V+5% / 440 mA

N12P-LP Total:40W (w/VRAM)

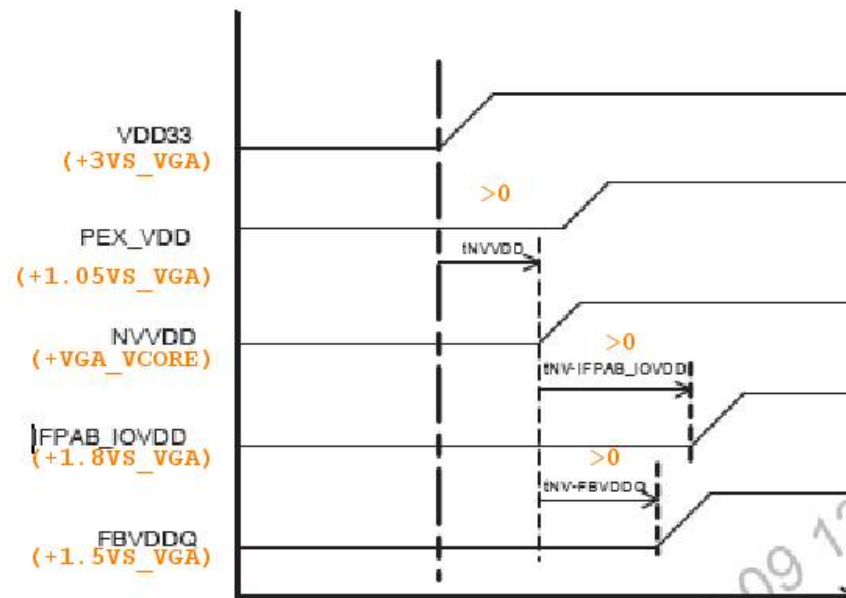
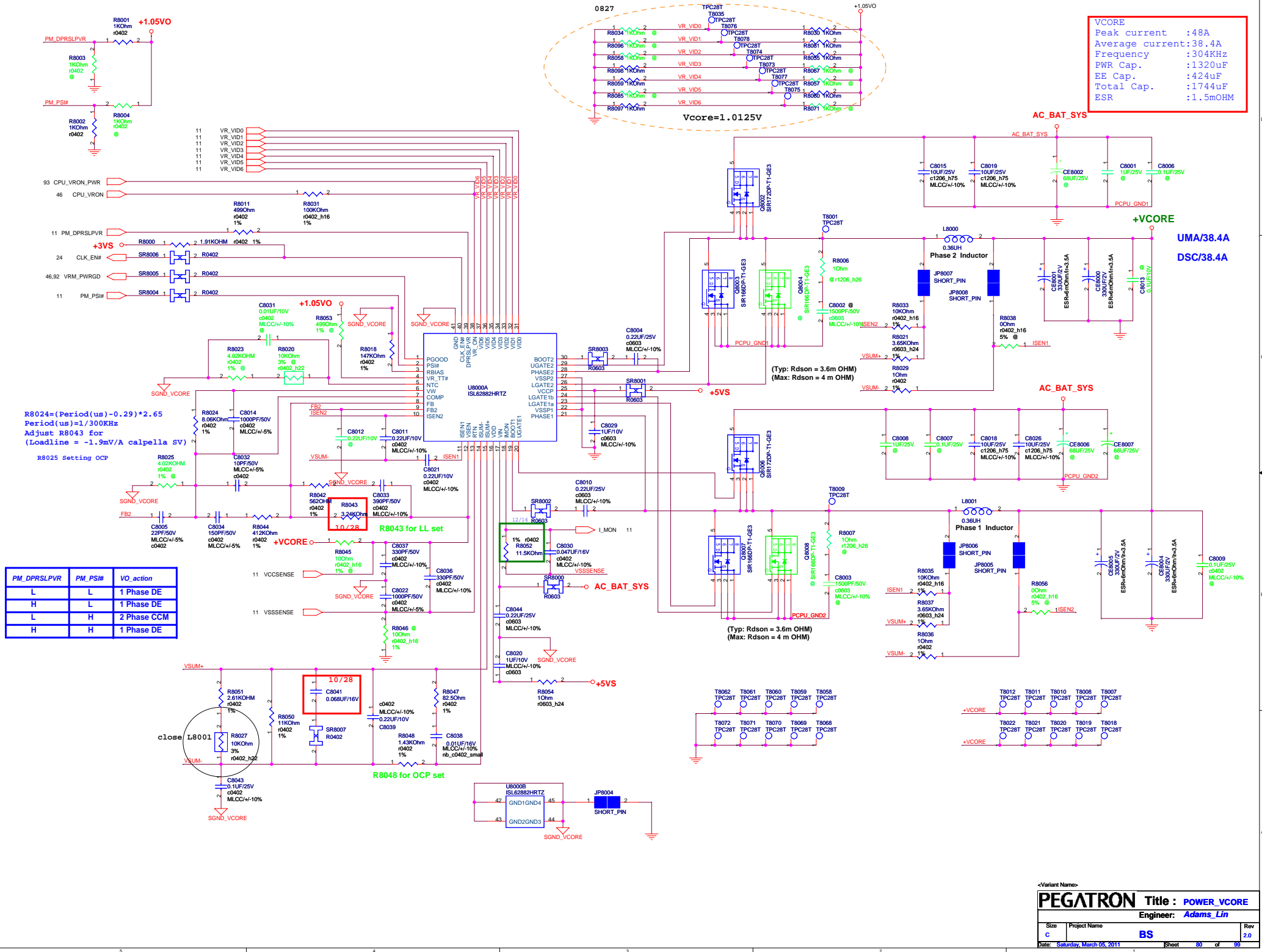


Figure 3.20 Recommended Power On Sequencing Order

Power Up Sequence :  
+3VS\_VGA -> +1.05VS\_VGA -> +VGA\_VCORE -> +1.5VS\_VGA -> +1.8VS\_VGA

Power Down Sequence :  
+1.8VS\_VGA -> +1.5VS\_VGA -> +VGA\_VCORE -> 1.05VS\_VGA -> +3VS\_VGA

according to Page 63, DG-05093-001\_v02



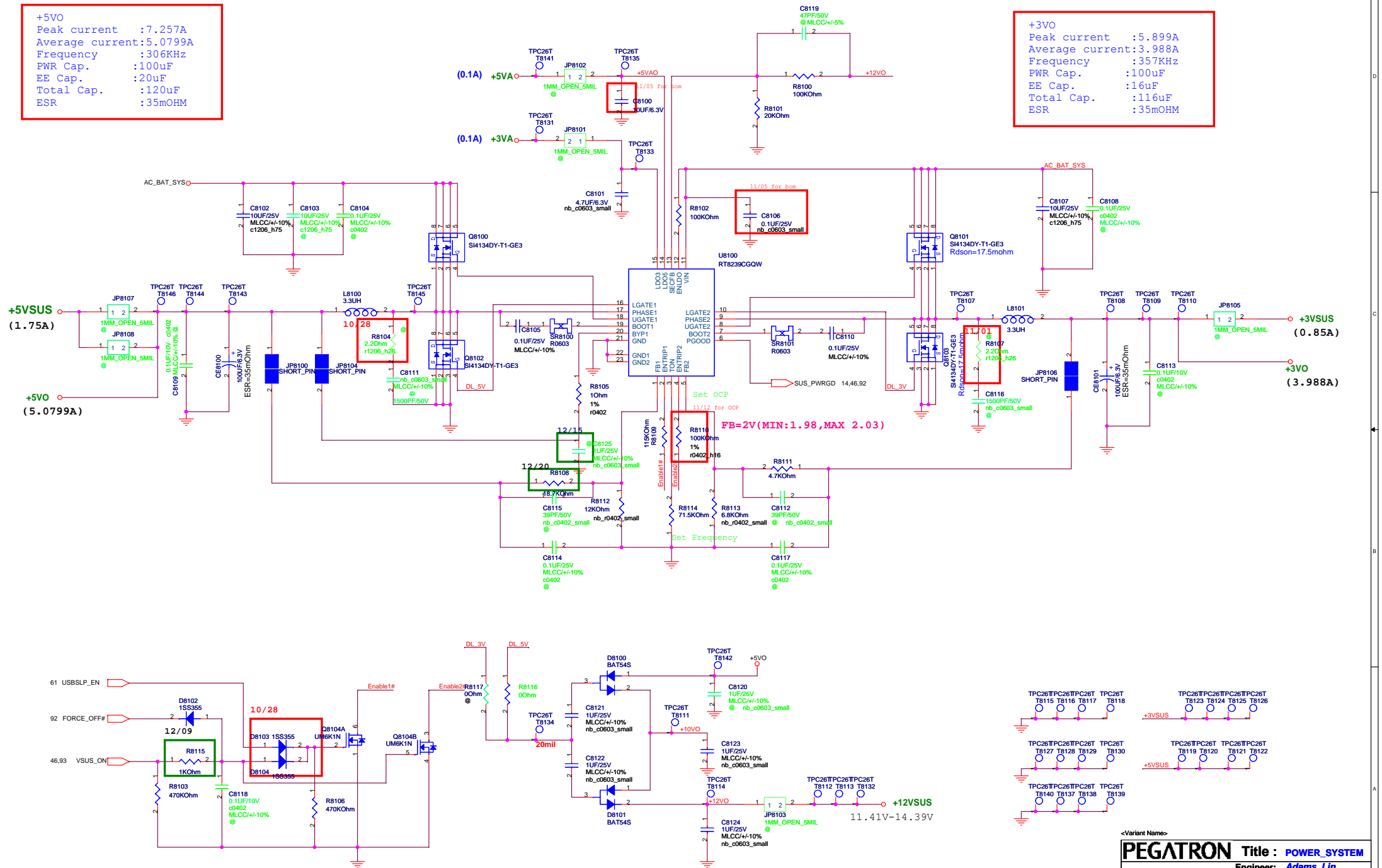
Vcore  
Peak current :48A  
Average current:38.4A  
Frequency :304KHz  
PWR Cap. :1320uF  
EE Cap. :424uF  
Total Cap. :1744uF  
ESR :1.5mOHM

$R8024 = (\text{Period(us)} - 0.29) * 2.65$   
 $\text{Period(us)} = 1 / 300\text{KHz}$   
Adjust R8043 for  
(Loadline = -1.9mV/A calpella SV)

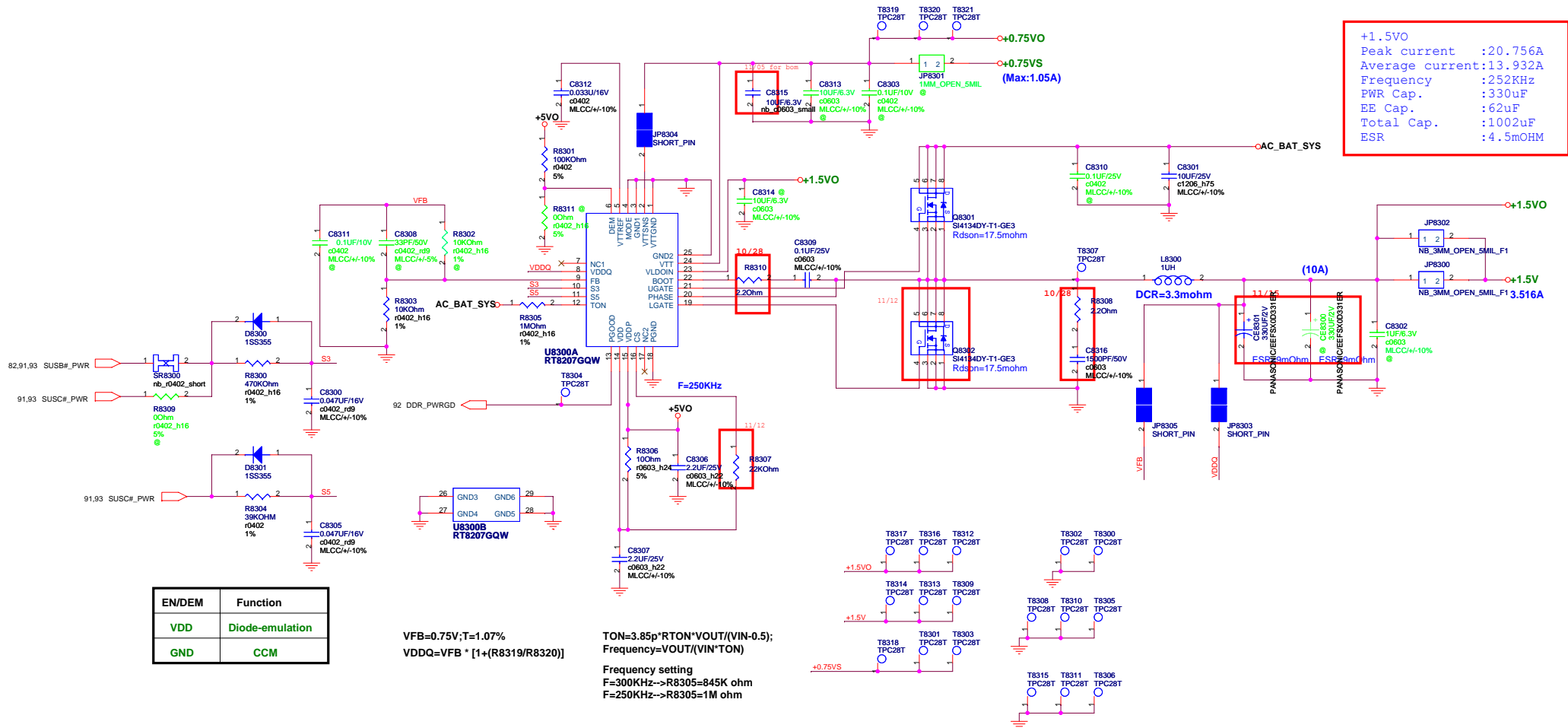
PM_DPRSLPVR	PM_PS#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

+5VO  
Peak current :7.257A  
Average current:5.0799A  
Frequency :306KHz  
PWR Cap. :100uF  
EE Cap. :20uF  
Total Cap. :120uF  
ESR :35mOHM

```
+3V0
Peak current      :5.899A
Average current:3.988A
Frequency         :357KHz
PWR Cap.         :100uF
EE Cap.          :16uF
Total Cap.       :116uF
ESR              :35mOHM
```







<Variant Name>

**PEGATRON** Title : **POWER\_DDR & VTT**

Engineer: **Adams\_Lin**

Size	Project Name	Rev
Custom	<b>BS</b>	2.0

Date: Saturday, March 05, 2011 Sheet 83 of 94



D

C

B

A

D

C

B

A

**<Variant Name>**

**PEGATRON** Title : POWER\_N/A

Engineer: *Adams\_Lin*

Size A	Project Name BS	Rev 2.0
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Date: Saturday, March 05, 2011 Sheet 85 of 94

5

4

3

2

1

5

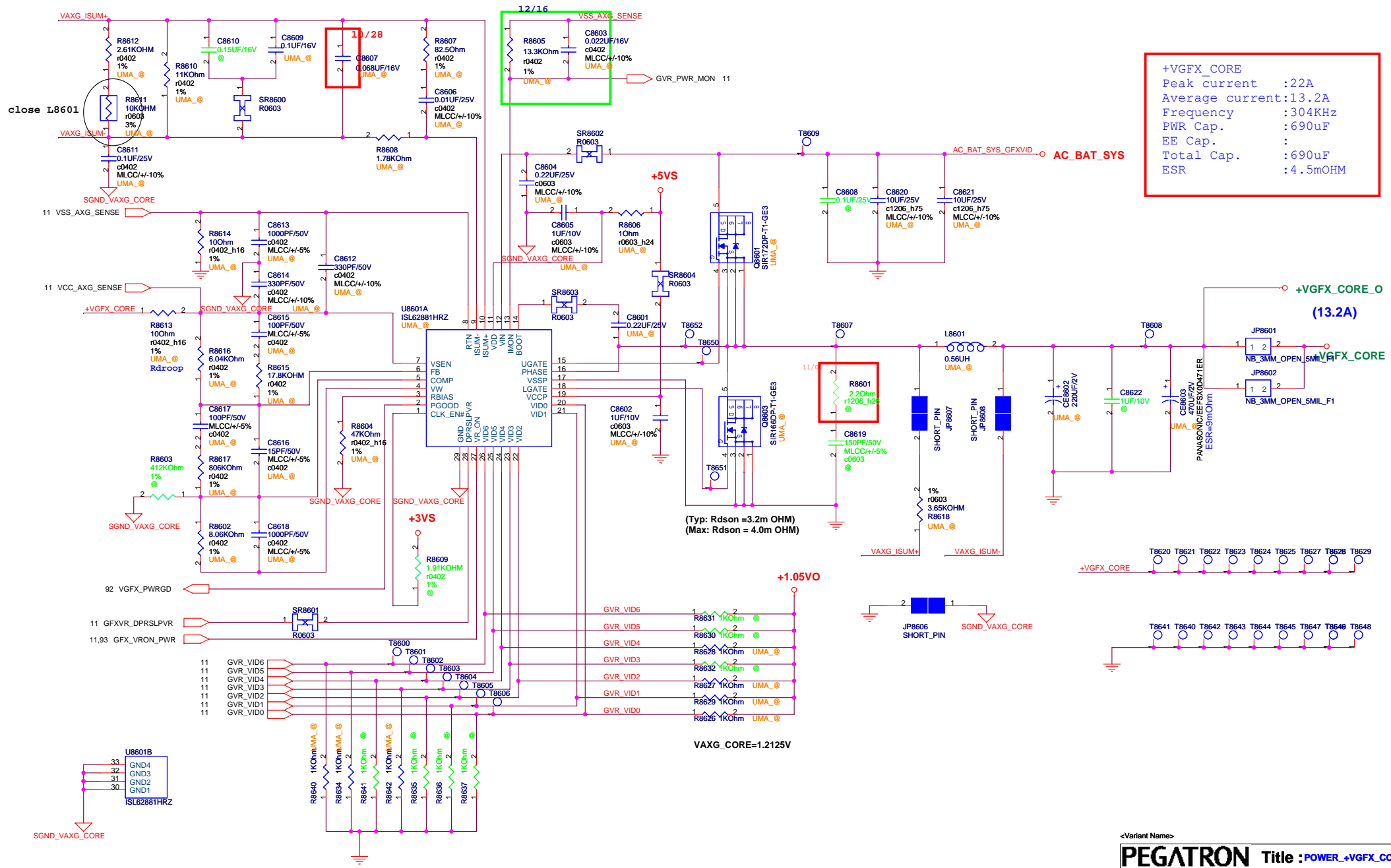
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4

3

2

1

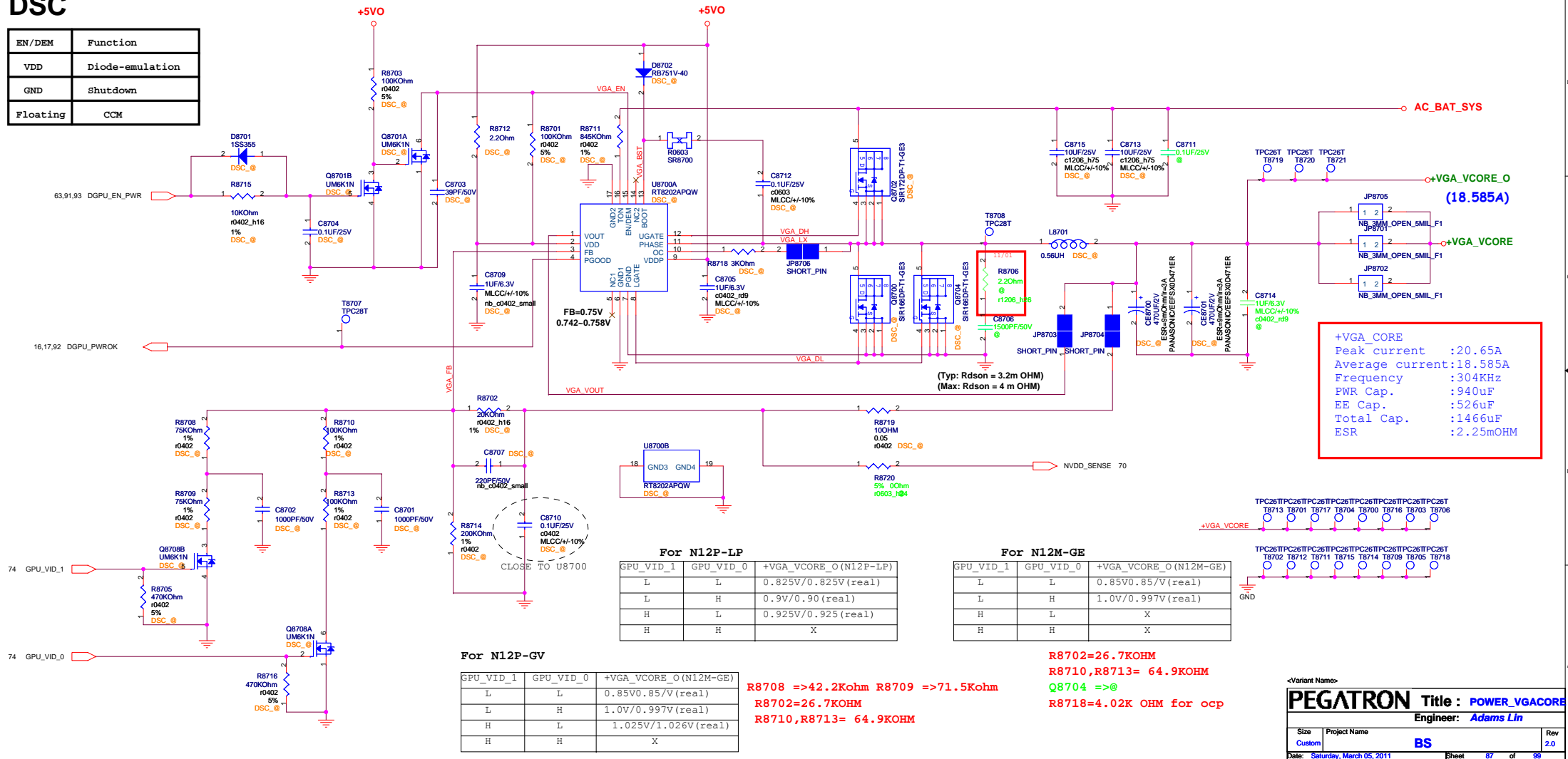


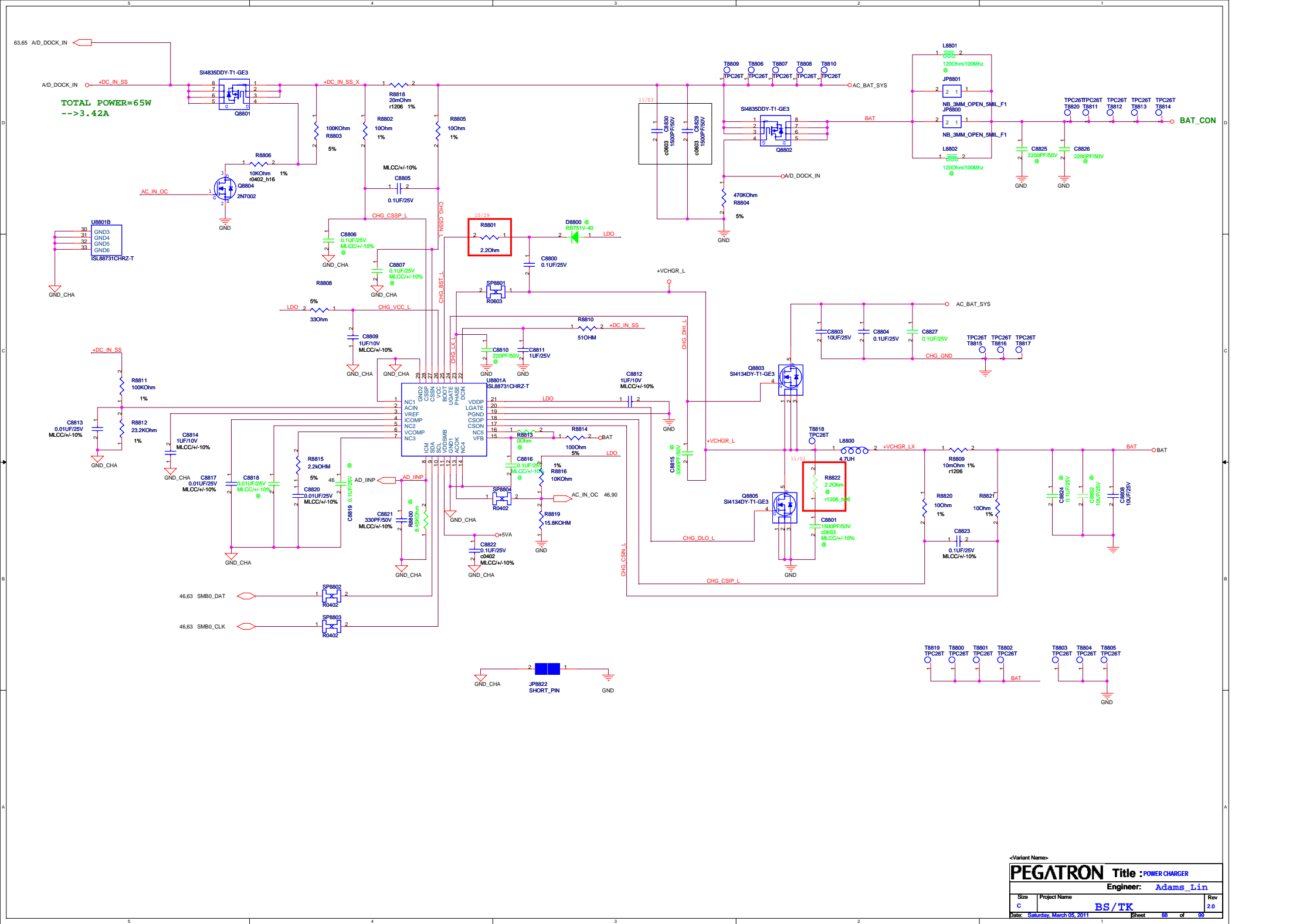
+VGFX\_CORE  
Peak current :22A  
Average current:13.2A  
Frequency :304KHz  
PWR Cap. :690uF  
EE Cap. :  
Total Cap. :690uF  
ESR :4.5mOHM



## DSC

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM





D

C

B

A

D

C

B

A

<Variant Name>

**PEGATRON** Title : **POWER\_N/A**

Engineer: *Adams\_Lin*

Size A	Project Name BS	Rev 2.0
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Date: Saturday, March 05, 2011 Sheet 89 of 94

5

4

3

2

1

5

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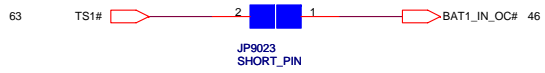
4

3

2

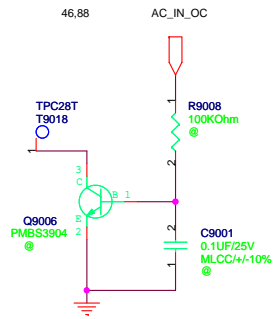
1

BATTERY IN DETECT

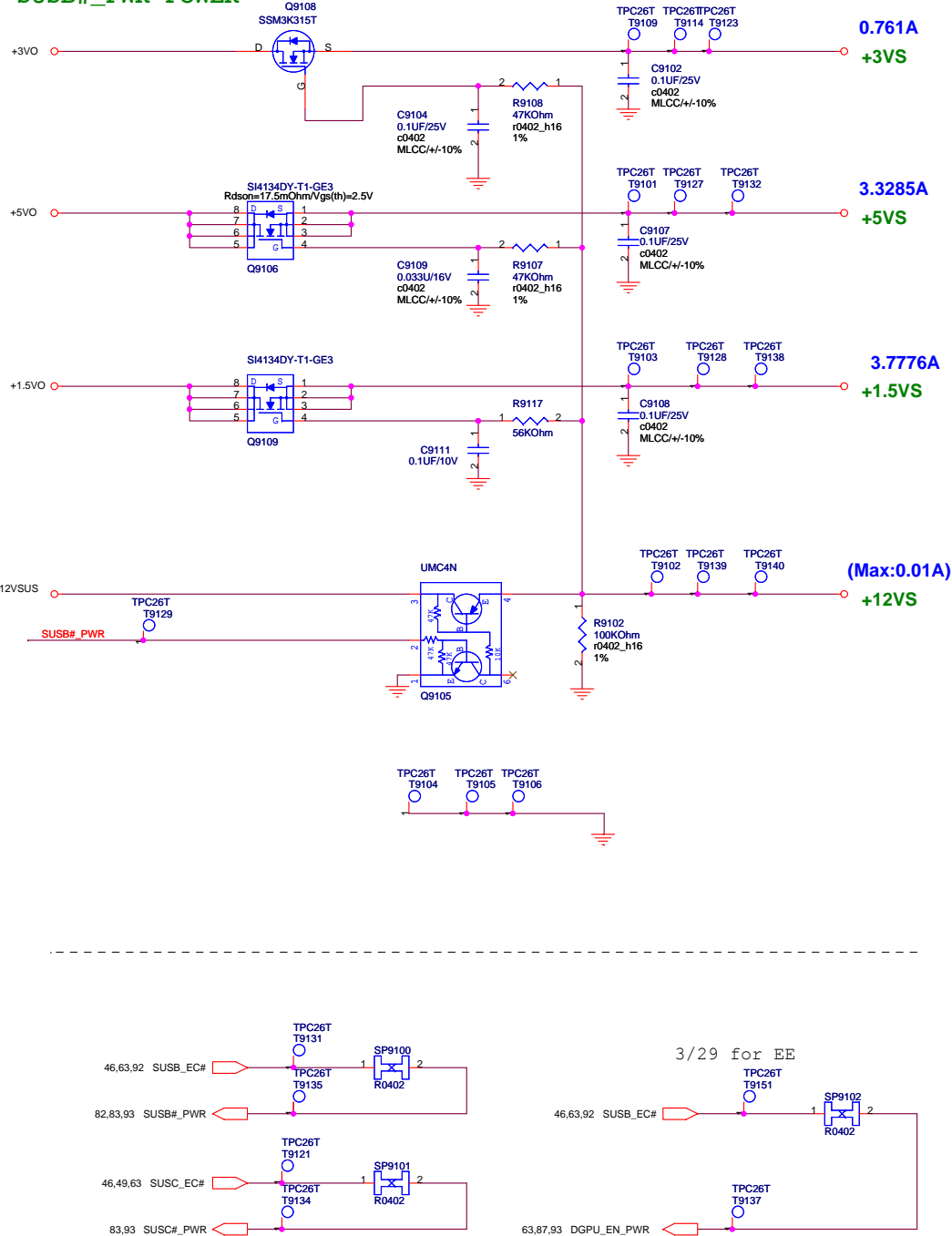


ADAPTER IN DETECT

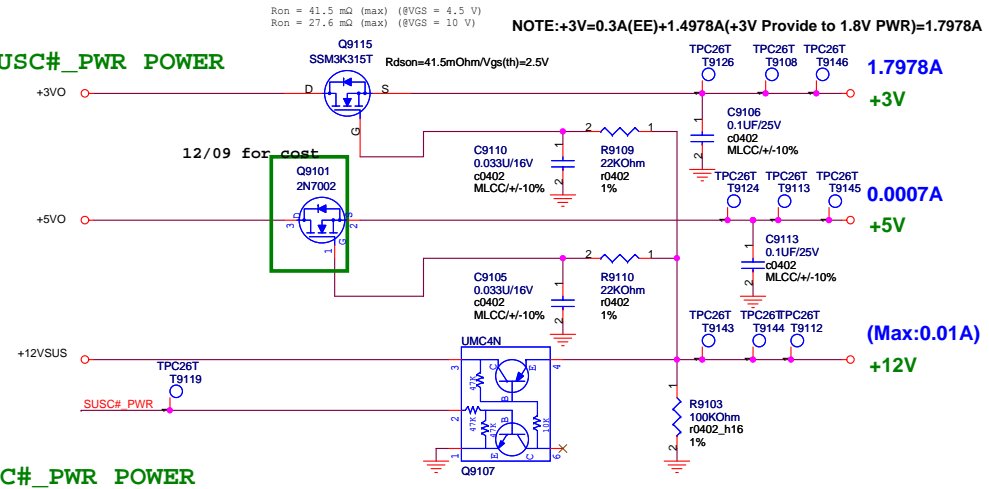
Use MAX17015 IC function to Cost down component



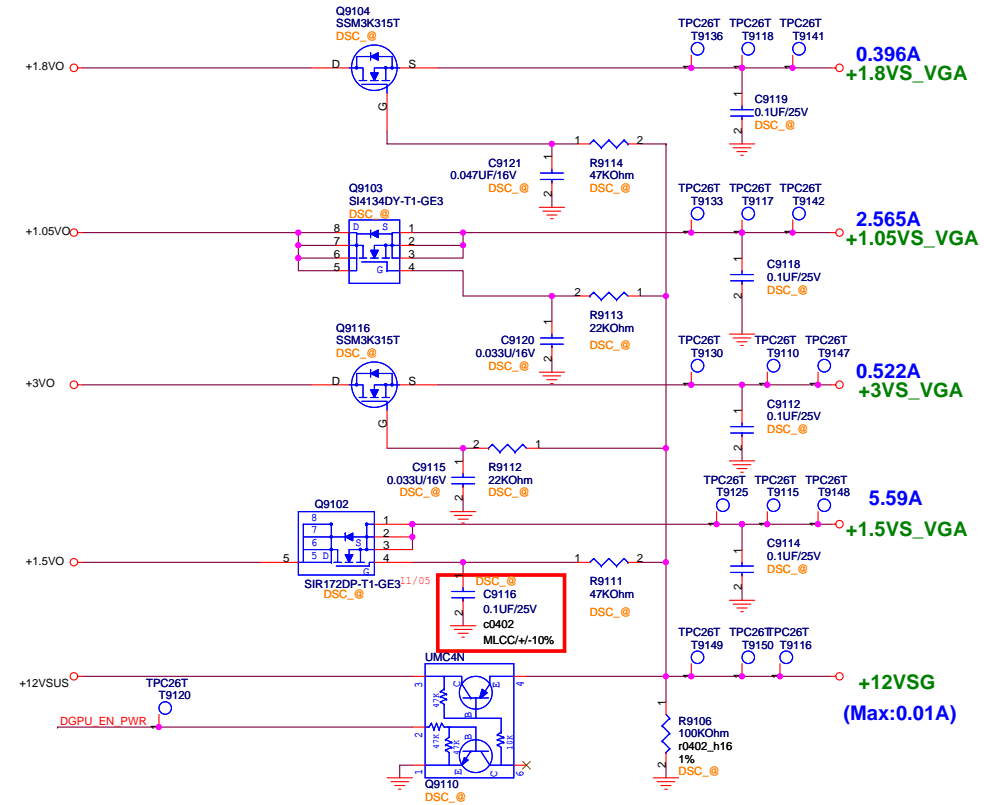
## SUSB#\_PWR POWER



## SUSC#\_PWR POWER



## DSC#\_PWR POWER



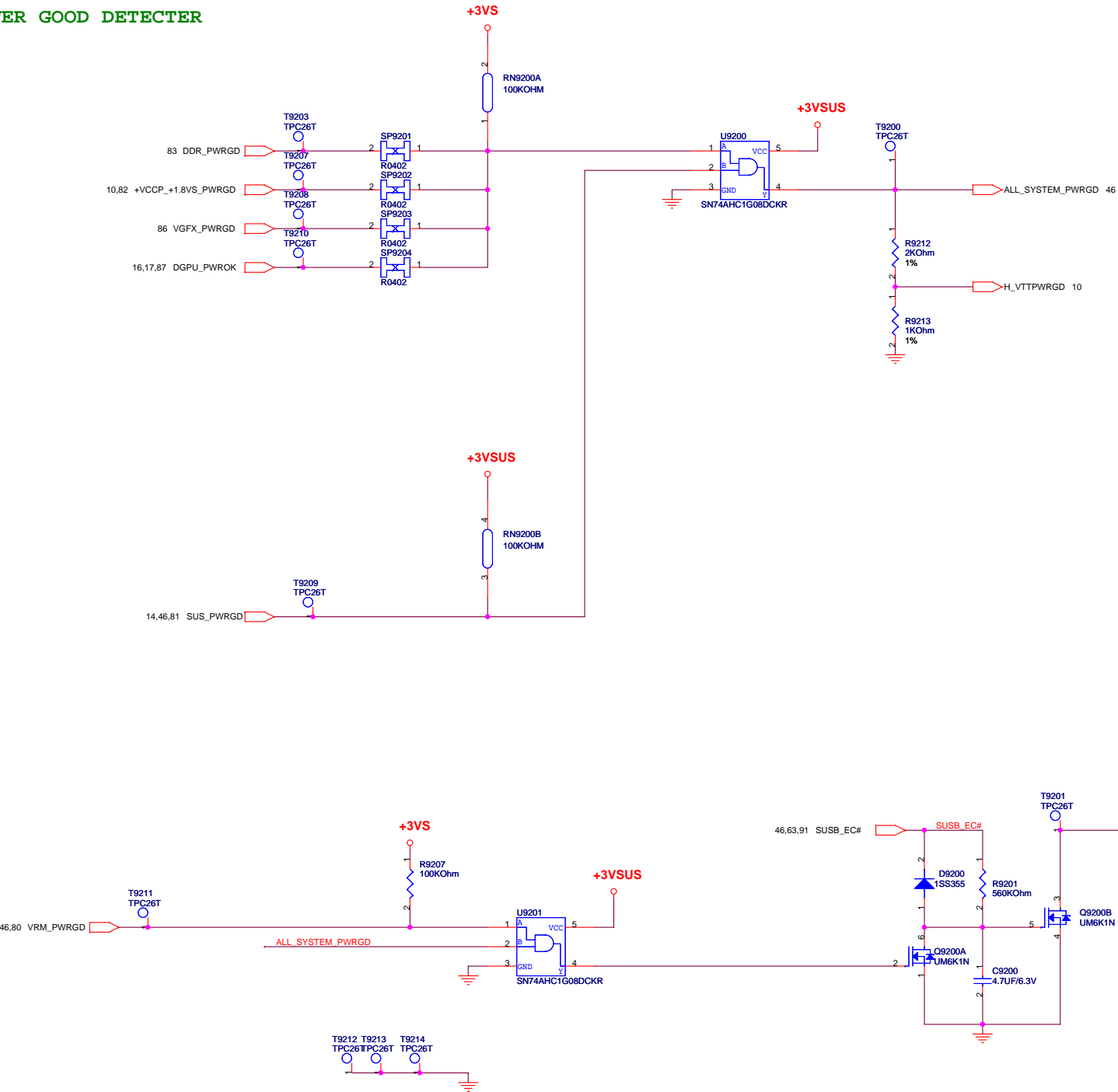
&lt;Variant Name&gt;

PEGATRON Title : POWER\_LOAD SWITCH

Engineer: Adams\_Lin

Size	Project Name	Rev
Custom	BS	2.0
Date: Saturday, March 05, 2011	Sheet 91 of 99	

POWER GOOD DETECTER



AC\_BAT\_SYS AC\_BAT\_SYS 37,80,81,82,83,86,87,88  
BAT\_CON BAT\_CON 63,88  
BAT BAT 88

+5VA +5VA 49,61,66,81,88  
+3VA +3VA 13,46,48,61,63,66,81

+5VO +5VO 81,82,83,87,91  
+3VO +3VO 81,91  
+1.8VO +1.8VO 82,91  
+1.5VO +1.5VO 83,91  
+1.05VO +1.05VO 80,82,86,91  
+VGFX\_CORE\_O +VGFX\_CORE\_O 86  
+VGA\_VCORE\_O +VGA\_VCORE\_O 87  
+0.75VO +0.75VO 83

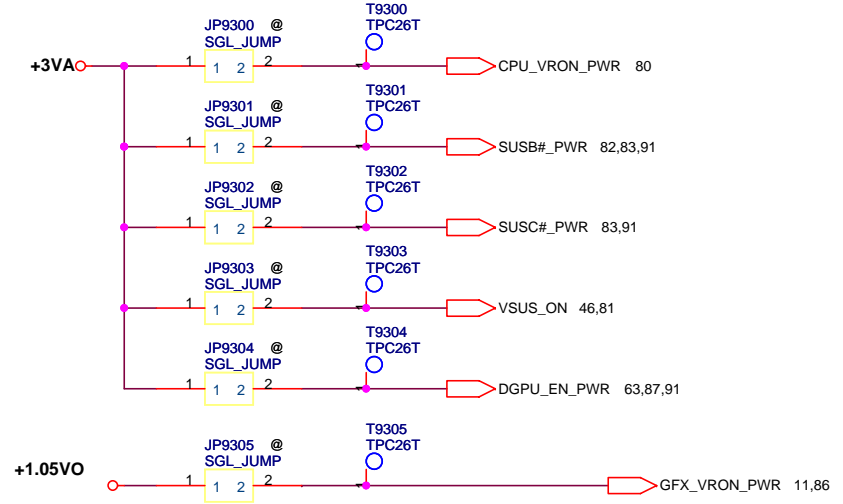
+12VS +12VS 38,39,91  
+5VS +5VS 15,19,38,39,41,44,46,48,49,60,63,66,80,86,91  
+3VS +3VS 10,13,14,15,16,17,18,19,21,22,24,32,37,39,41,42,44,45,46,48,60,63,65,66,67,80,86,91,92  
+1.8VS +1.8VS 11,18,19,82  
+1.5VS +1.5VS 10,11,24,55,63,91  
+0.75VS +0.75VS 21,22,63,83

+12VSUS +12VSUS 81,91  
+5VSUS +5VSUS 19,61,66,81  
+3VSUS +3VSUS 10,13,14,15,16,17,18,19,46,55,67,81,92

+12V +12V 91  
+5V +5V 63,66,91  
+3V +3V 37,50,63,65,82,91  
+1.5V +1.5V 10,21,22,63,83

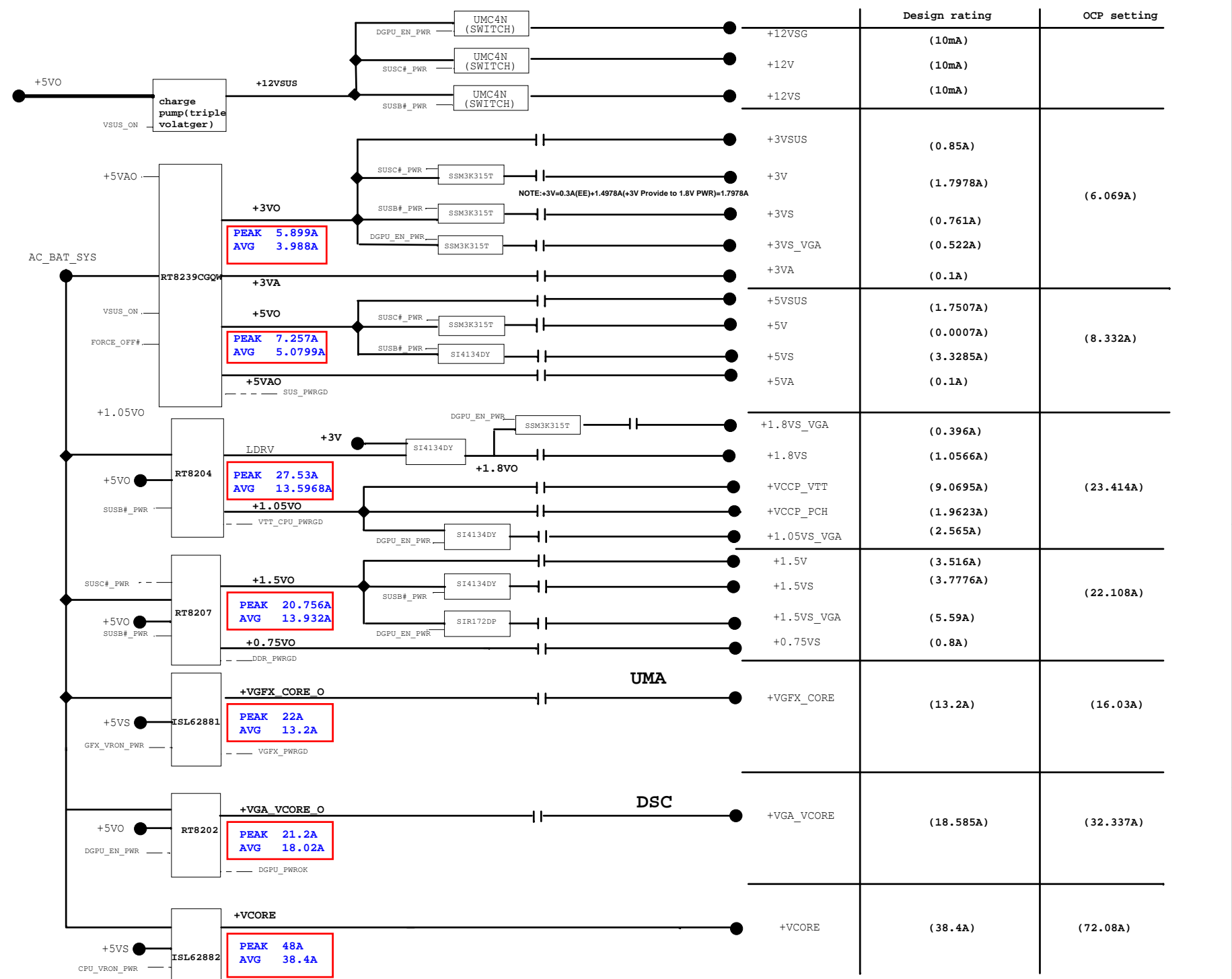
+VGA\_VCORE +VGA\_VCORE 63,75,87  
+VGFX\_CORE +VGFX\_CORE 11,86  
+VCORE +VCORE 11,12,80  
+12VSG +12VSG 91  
+3VS\_VGA +3VS\_VGA 70,72,73,74,91  
+1.8VS\_VGA +1.8VS\_VGA 63,73,91  
+1.5VS\_VGA +1.5VS\_VGA 63,71,76,77,91  
+1.05VS\_VGA +1.05VS\_VGA 63,70,71,72,73,91

## FOR POWER TEST



<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Adams_Lin	
Size Custom	Project Name BS		Rev 2.0
Date: Saturday, March 05, 2011		Sheet	93 of 94





modify notice

Version	Date	Description
2.0	1121	add test points:T8149 T8147 T8136 T8148 T8151 T8152 T8150 T8153 T8820 T8819
1.1	1019	